Data acquisition system of the highly granular time-of-flight neutron detector of the BM@N experiment at the NICA accelerator complex

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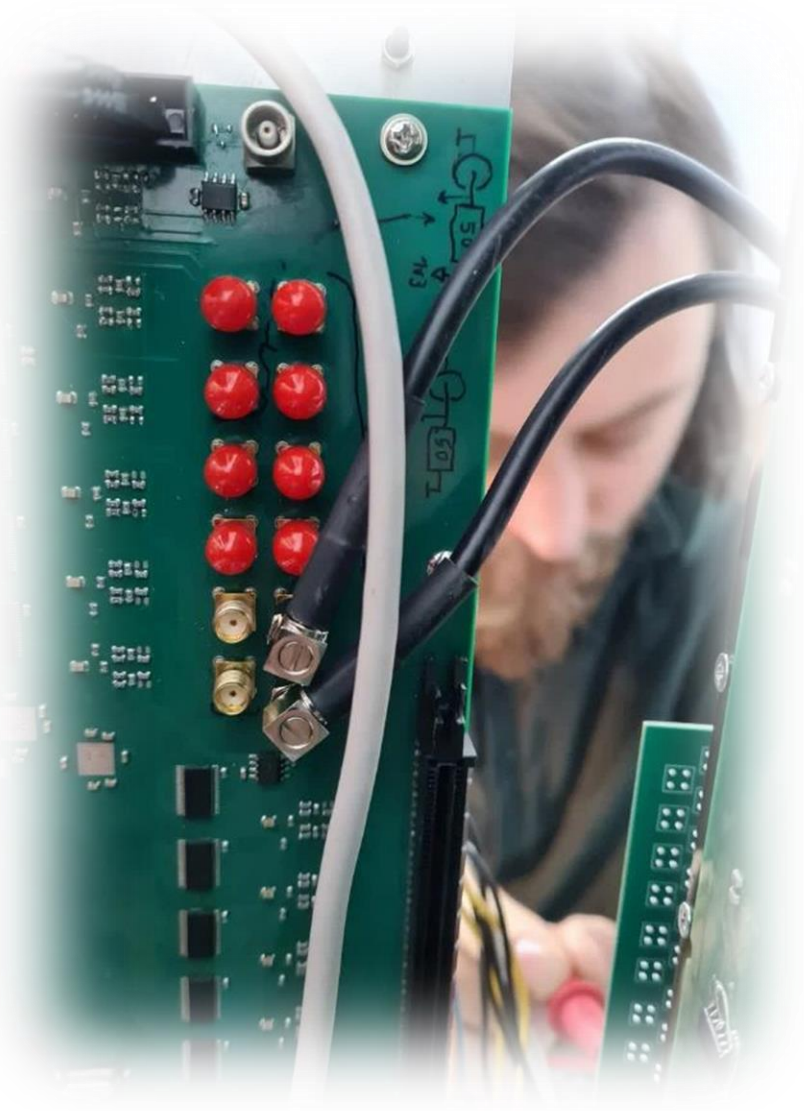
July 5, 2024

Outline

- *HGND detector overview*
- *HGND readout topology*
- *100ps FPGA based TDC*
- *FEE development and tests*



Others HGND reports:

311. Graph Neural Network-based neutron reconstruction in the HGND at the BM@N experiment
Vladimir Bocharnikov (HSE University)
01.07.2025, 18:20

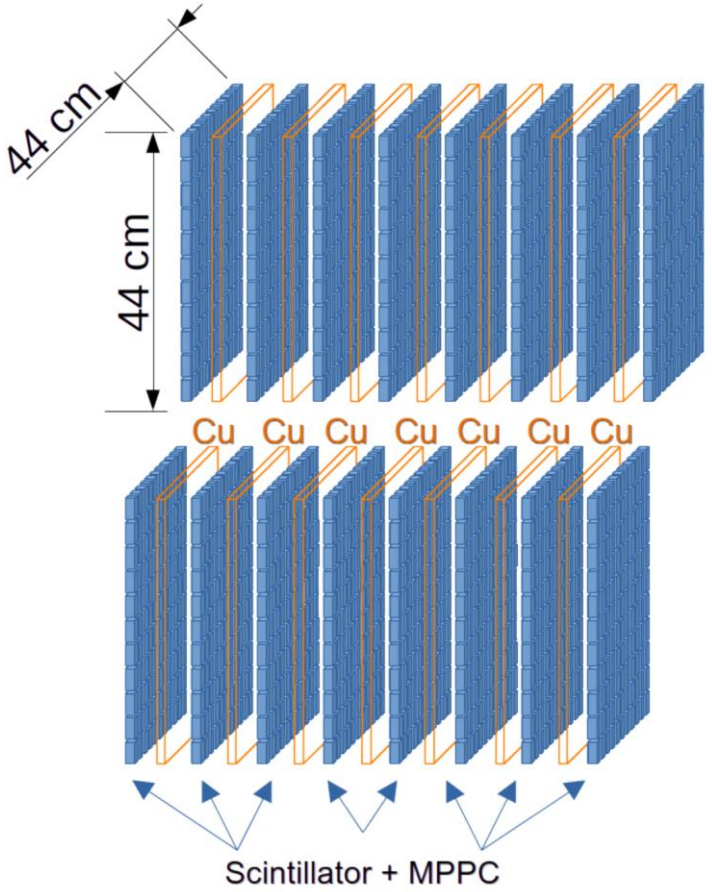
286. Development of the method of reconstruction of neutron energy spectrum with HGND in the BM@N experiment
Arseniy Shabanov (INR RAS; MIPT)
03.07.2025, 16:40

217. Measurement of neutron yields in the Xe+CsI reaction by the Highly Granular time-of-flight Neutron Detector prototype in the BM@N experiment
Aleksandr Zubankov (Institute for Nuclear Research of the Russian Academy of Sciences)
05.07.2025, 12:10

The highly granular time-of-flight neutron detector: HGND

- The HGND is intended to measure ***azimuthal neutron flow and neutron yields*** in nucleus-nucleus interactions in heavy-ion collisions with energies up to 4A GeV in the fixed target experiment BM@N at JINR.
- To study the dependence of the equation of state of nuclear matter on the term characterizing the isospin (proton-neutron) asymmetry of nuclear matter
- No neutron flow data at the energy range of the BM@N so far.
- These data will be important to astrophysics: the relation of mass of neutron stars and its radius depends of EoS

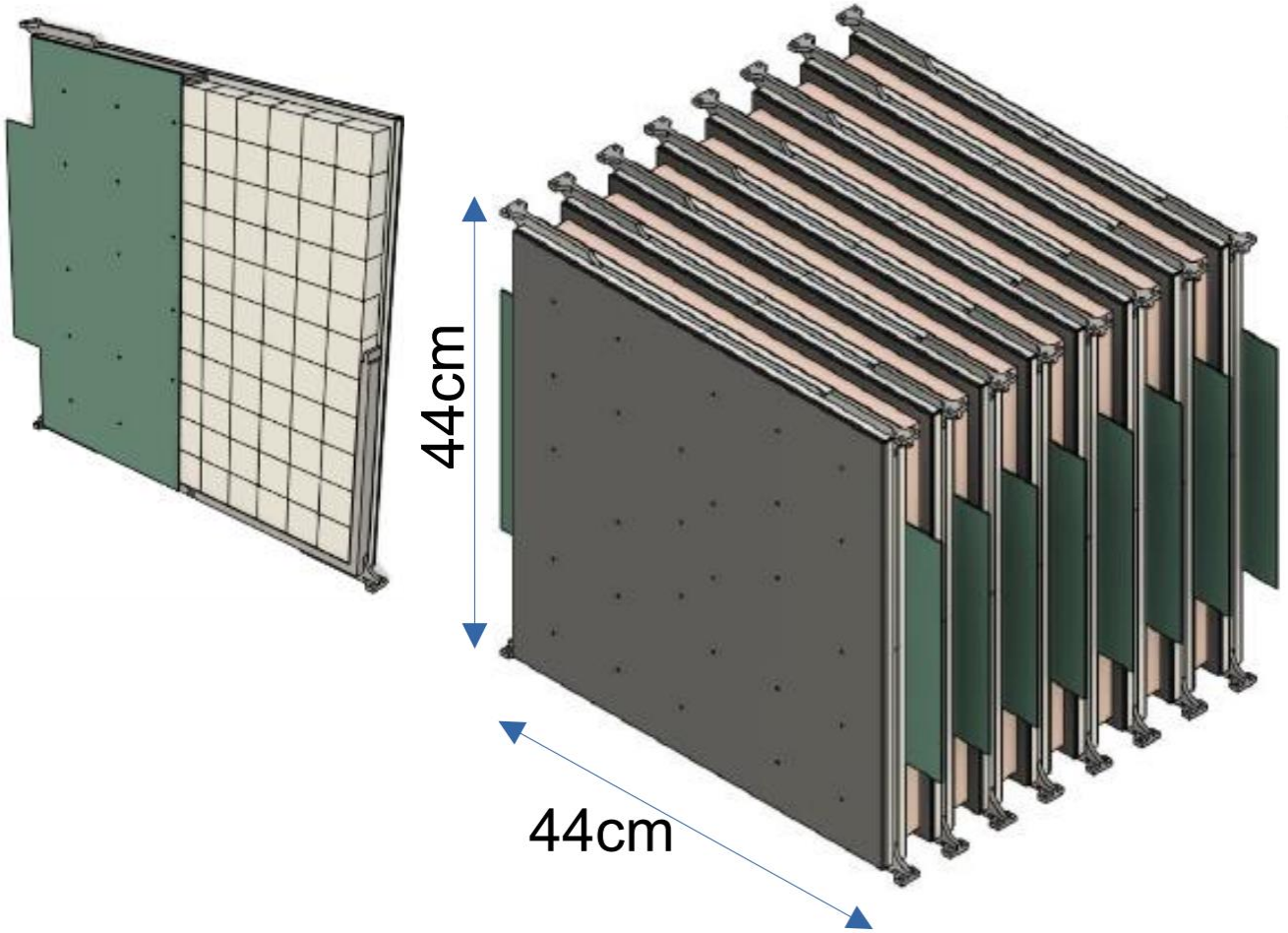
- (2x) 8 layers:
  - 3cm Cu (absorber)
  - 2.5cm Scintillator
  - 0.5cm PCB
  - Transverse size: 44x44 cm2
  - 11x11 scintillator cell grid



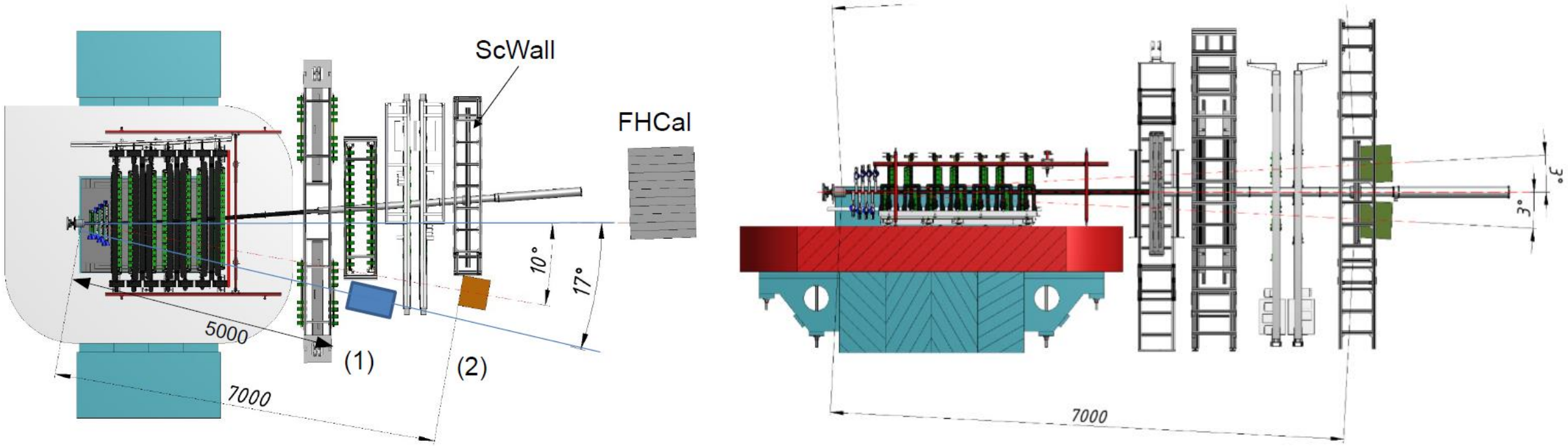
The highly granular time-of-flight neutron detector: HGND

- **EQR15 11-6060D-S MPPC**
  - active aria 6x6 mm²
  - quantum efficiency of 45% (420 nm)
  - gain of approximately 4×10^5

- polystyrene-based **scintillators** POPOP decay time 3.9±0.7 ns.
- Cell time resolution 150ps
- Nuclear interaction length: ~0.5m, ~1.5 λin
- Neutron detection efficiency: ~50% @ 1 GeV
- Energy resolution: - 2% (0.3 GeV); 20% (4 GeV)
- MIP light output value of 158±9 ph.e.
- Dynamic range: 1 – 8 MIP

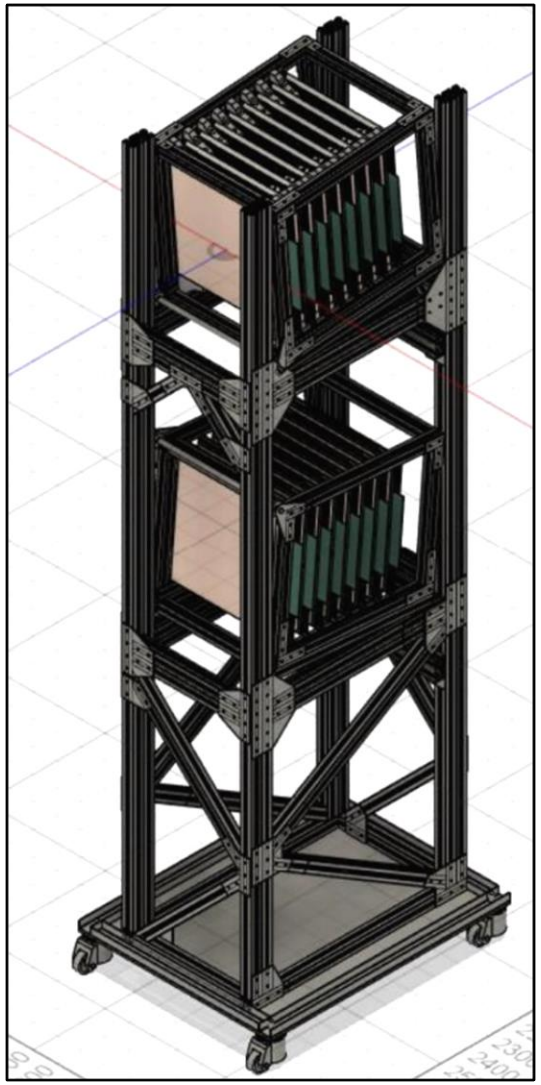


Planned location of the stand with 1 HGND module at the next session on BM@N



- ToF method with T0 as the “start” signal source
- 7m measurement distance
- Detector is split into 2 “blocks” for improved acceptance

The HGND mechanical layout

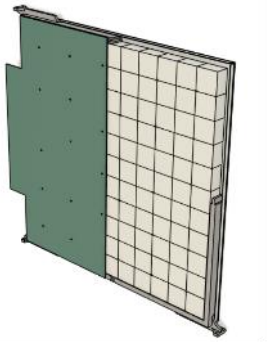


HGND mechanical: design (left) and support assembled at INR (right)

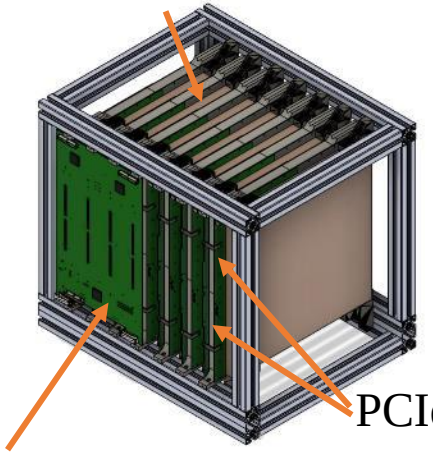
The HGND support was installed at BM@N line for the upcoming beam tests

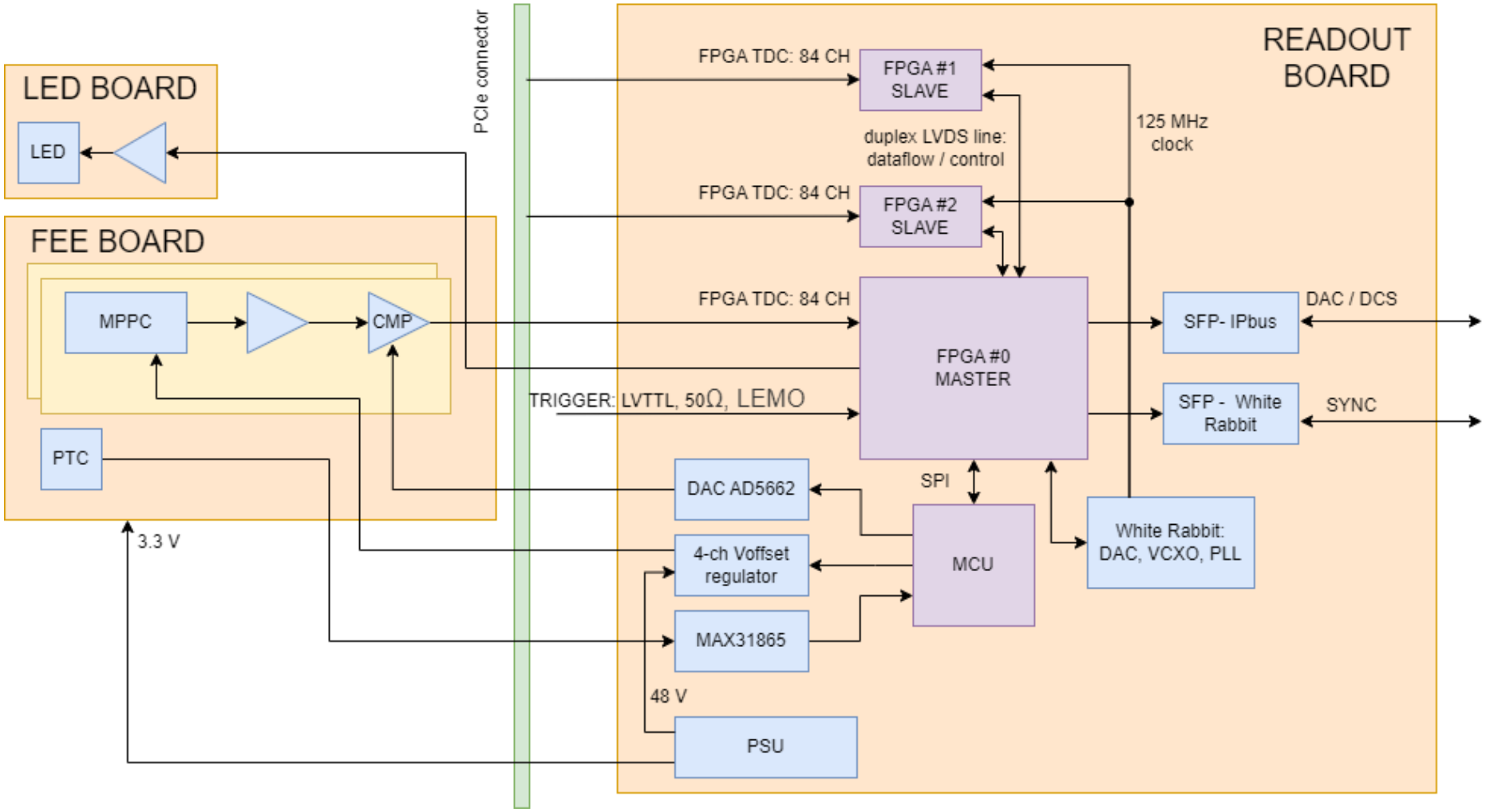
FEE & readout architecture

- 16 layers with scintillation matrix 11X11
- 16 LED boards
- 32 FEE boards
- 8 Readout boards
- 3 FPGA per board
- 84 channels per FPGA
- 2000 channels in total

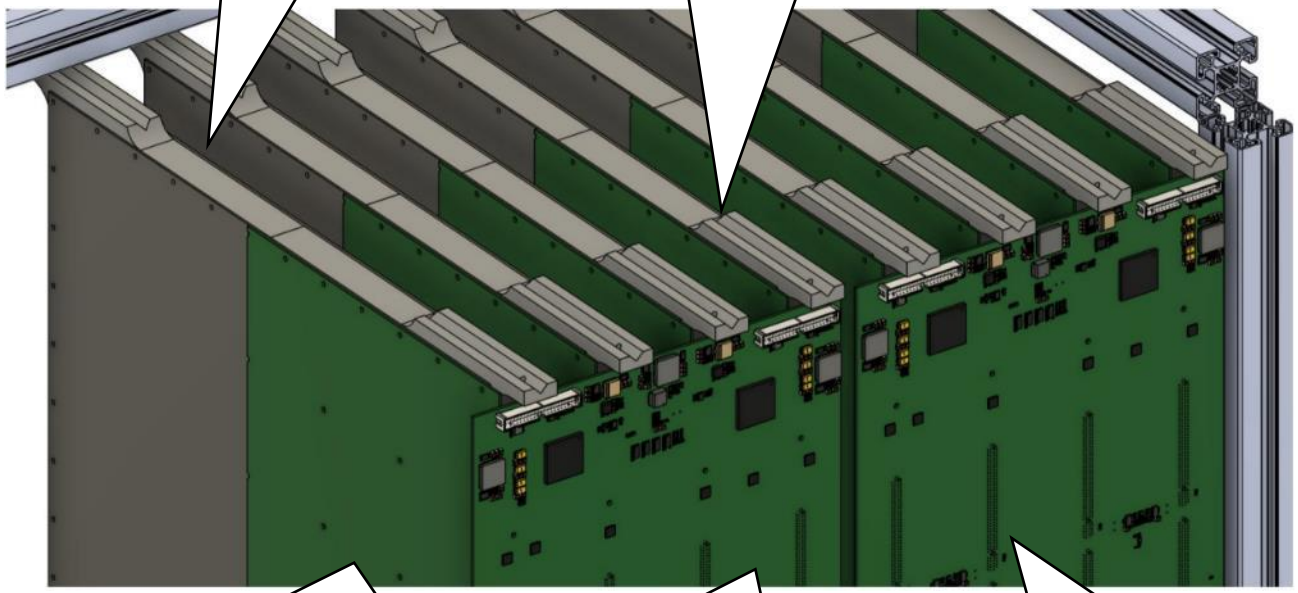


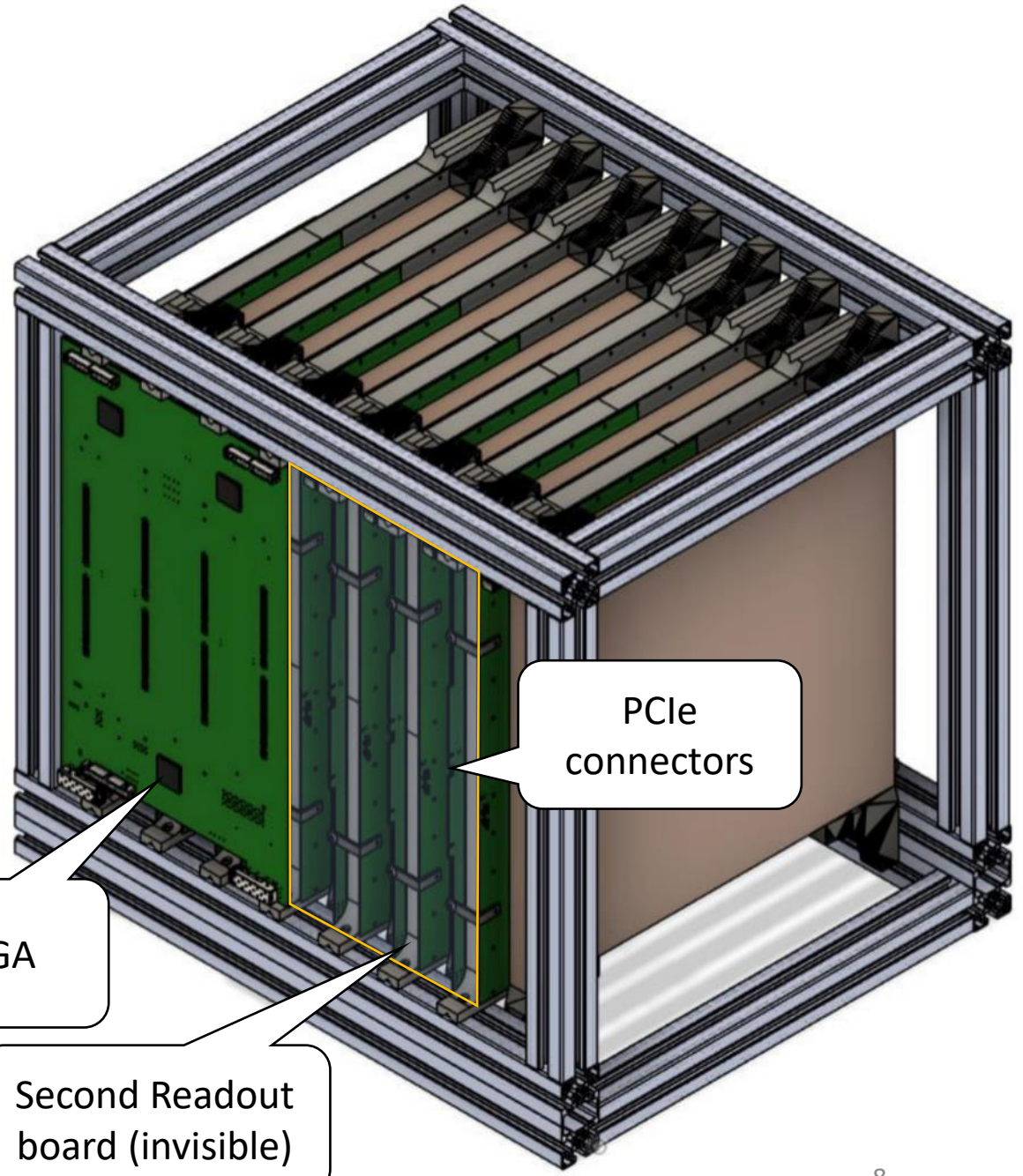
FEE board





FEE & readout board: close-up





Readout & trigger

- ***100 ps*** TDC is implemented in Kintex 7 FPGA, 84 channels per FPGA chip (2000 total)
- ***White Rabbit*** (WR) is used for event's time synchronization (8 links total):
  - TDCs use clock sourced from WR synchronous to whole BM@N
  - WR timestamps are assigned to measured events

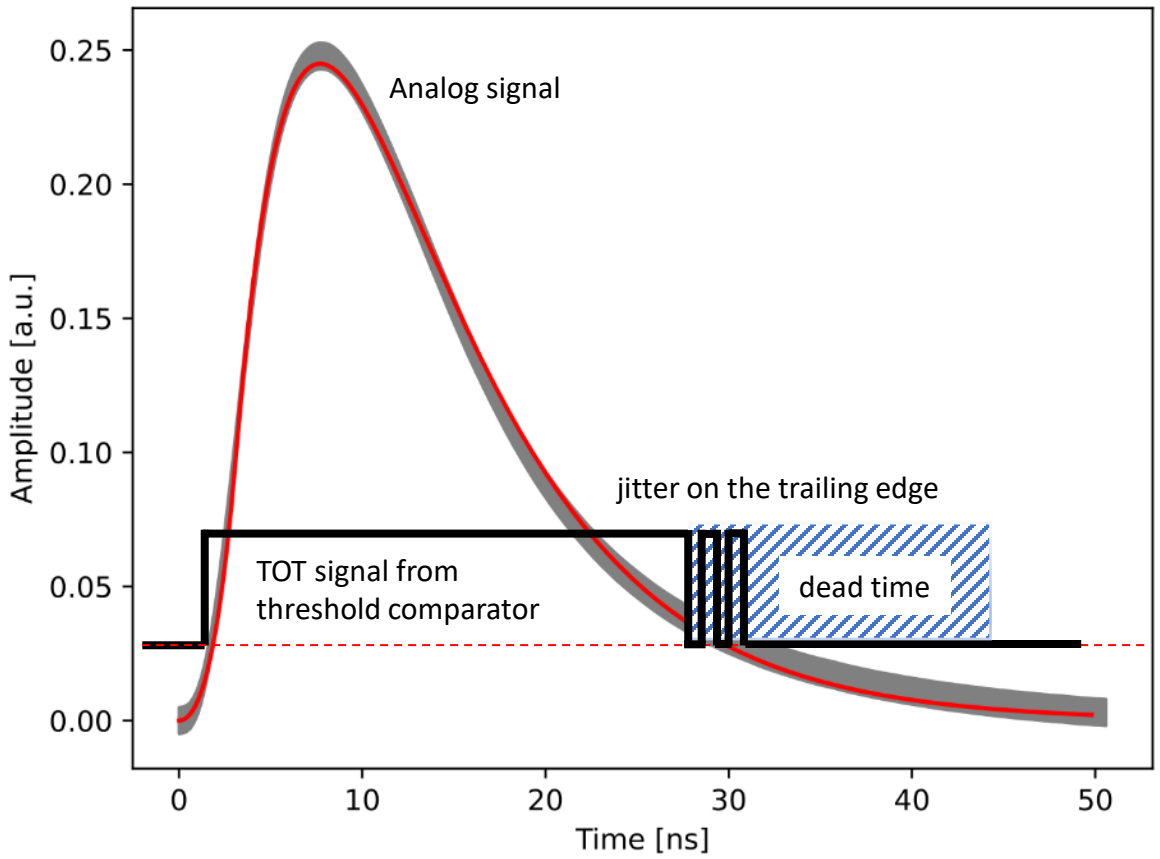
- Ethernet UDP protocol (***IPbus*** [1]) is used for data forwarding and board control
- Local network connect readout boards (8 ethernet links) with FLP

- The maximum HGND channel load is 3 kHz. The event size is 7x16 bits. The upper limit per link is not exceed ***100 Mbit/s***. ***The continuous readout*** is implemented without busy signal.

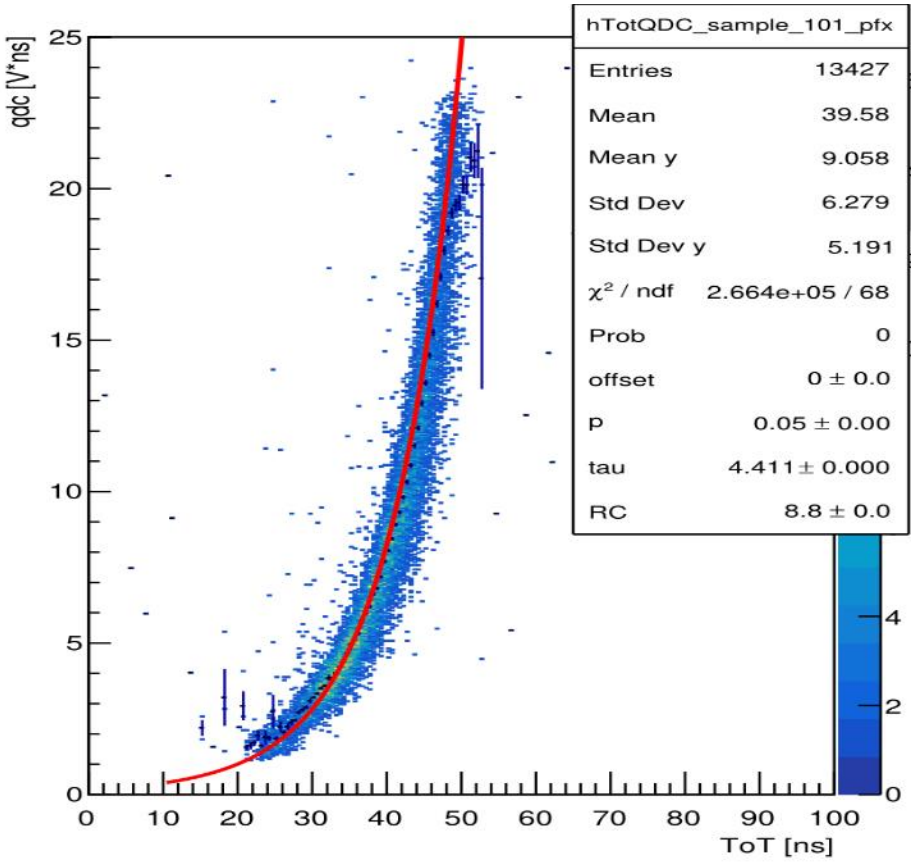
- The trigger is processed on FLP site:
  - Trigger signal is connected to TDC channel and digitized with WR timestamp in FPGA
  - Message trigger accompanied by a timestamp is transmitted to FLP for event selection

[1] C. Ghabrous Larrea, K. Harder, D. Newbold, D. Sankey, A. Rose, A. Thea and T. Williams, ***IPbus: a flexible Ethernet-based control system for xTCA hardware***, *JINST 10 (2015) no.02, C02019.*

TDC Time Over Threshold (TOT)



Amplitudes vs TOT time with analytical forecast



TOT amplitude resolution is in range 14 - 22%

- The threshold is tunable around 20 mV
- Signals length range is 20 – 60 ns
- Signals less than 6.4 ns are rejected for noise reduction
- Dead time is tunable in range 30 – 200 ns for comparator jitter filtering
- Minimum TOT time and dead time available in FPGA TDC are 3.2 ns

Tapped Delay–Line (TDL) FPGA based TDC

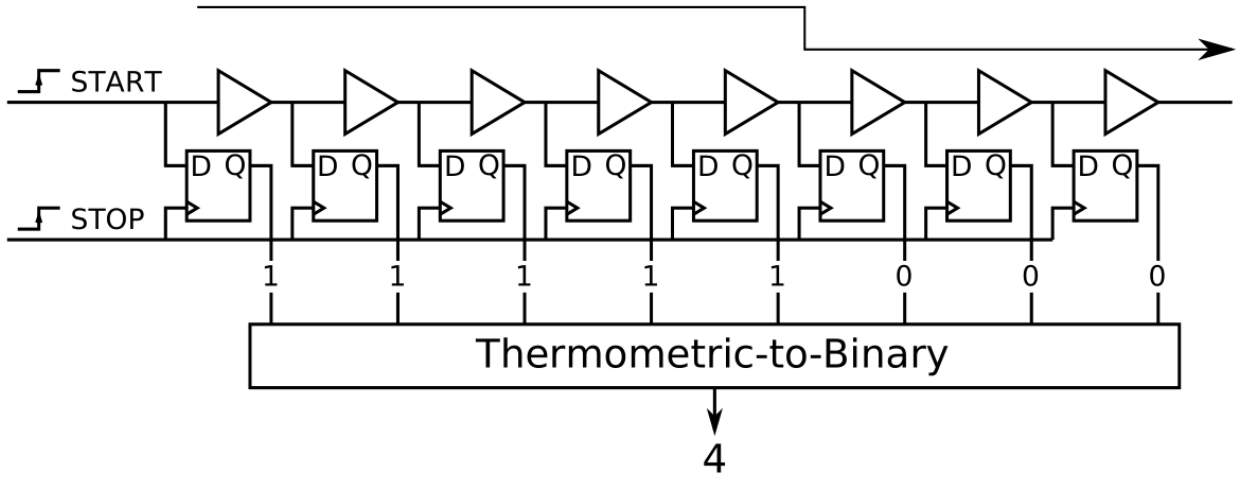
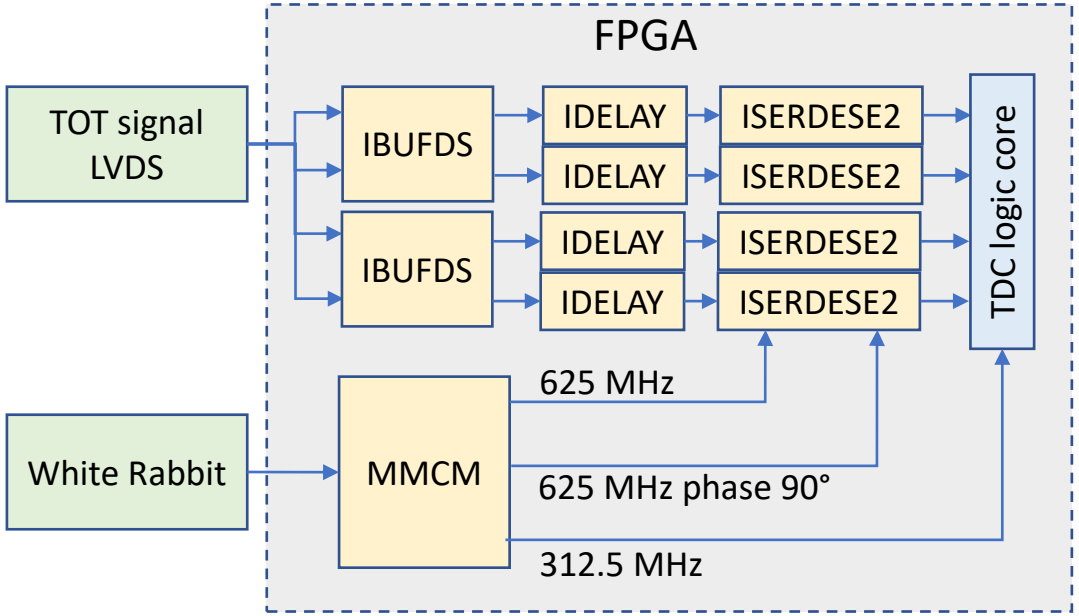


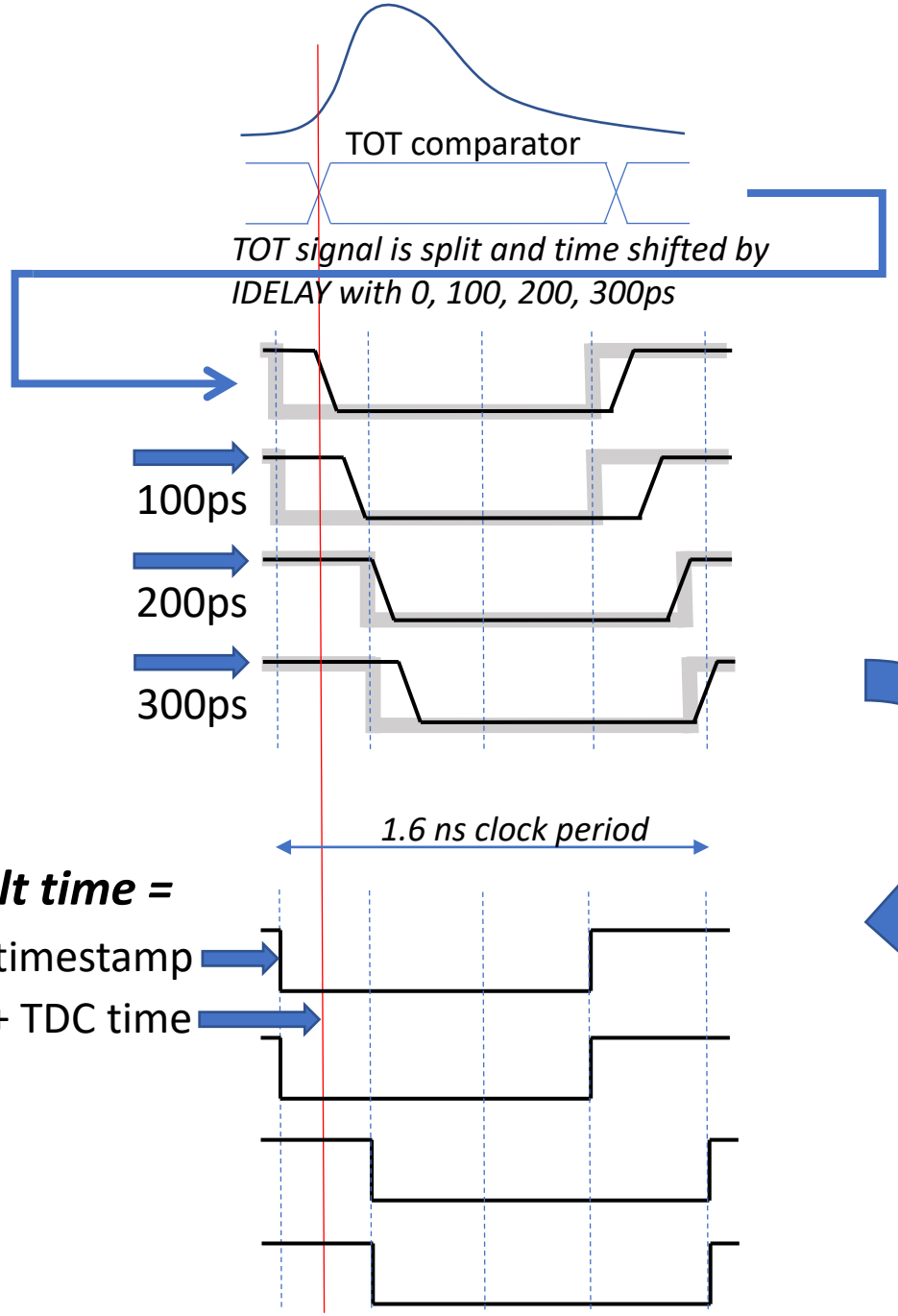
FIGURE 1. TDL and structure coding the time distance between START and STOP edges into a binary number.

- Time resolution up to 3.5 ps
- High FPGA resource utilization
- Temperature and FPGA design calibration dependance

[2] F. GARZETTI et al. “Time-to-Digital Converter IP-Core for FPGA at State of the Art” DOI 10.1109/ACCESS.2021.3088448

The 100ps FPGA TDC principle of operation

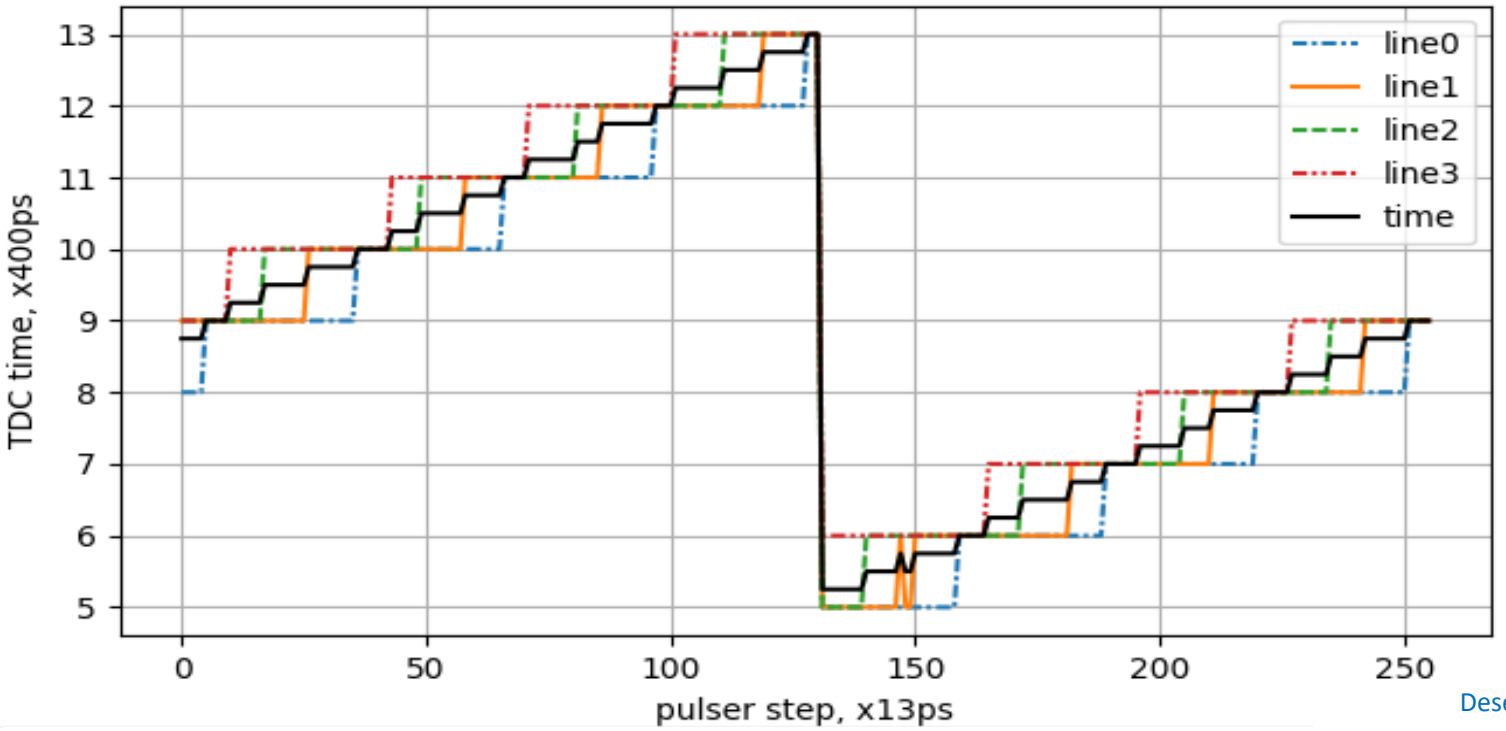


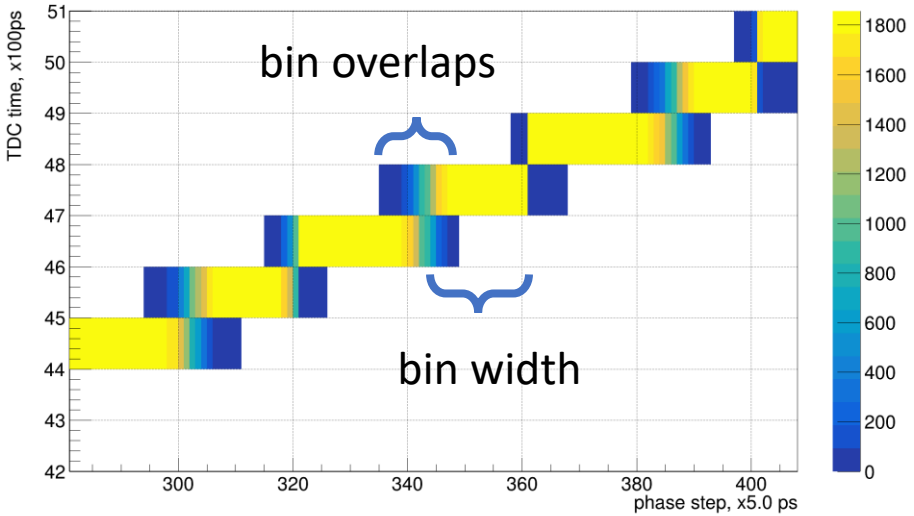


The TDC is **based on the Kintex-7** input serial-to-parallel converter with oversampling capability and programmable delay. The design is **based on Xilinx recommendations**, and uses **only documented features** of the FPGA within its specifications.

[3] D. Finogeev, F. Guber, A. Izvestnyy, N. Karpushkin, A. Makhnev et al., ***Development of 100 ps TDC based on Kintex 7 FPGA for the High Granular Neutron Time-of-Flight detector for the BM@N experiment,*** *DOI: 10.1016/j.nima.2023.168952*

The FPGA TDC time scan results

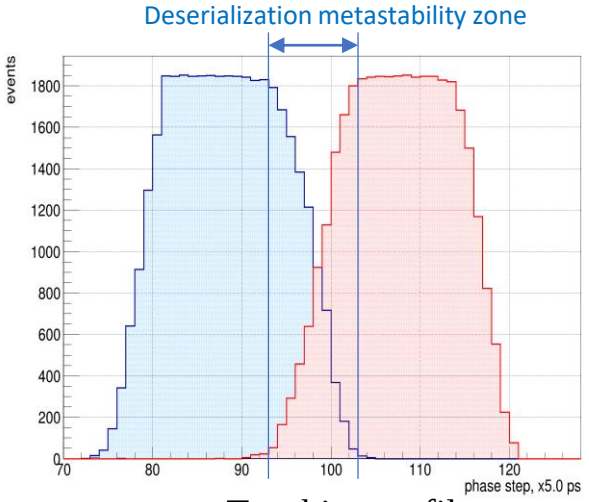




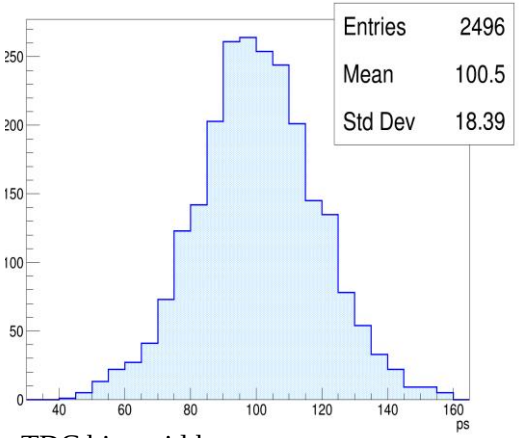
The TDC time dependence on pulse time shift.

Four TDC lines and the resulting time dependence on the pulse time shift are shown.

- TDC bins width std dev: 18 ps
- Deserialization metastability zone (mean) is 65 ps (on the level 1 events)



Two bins profile

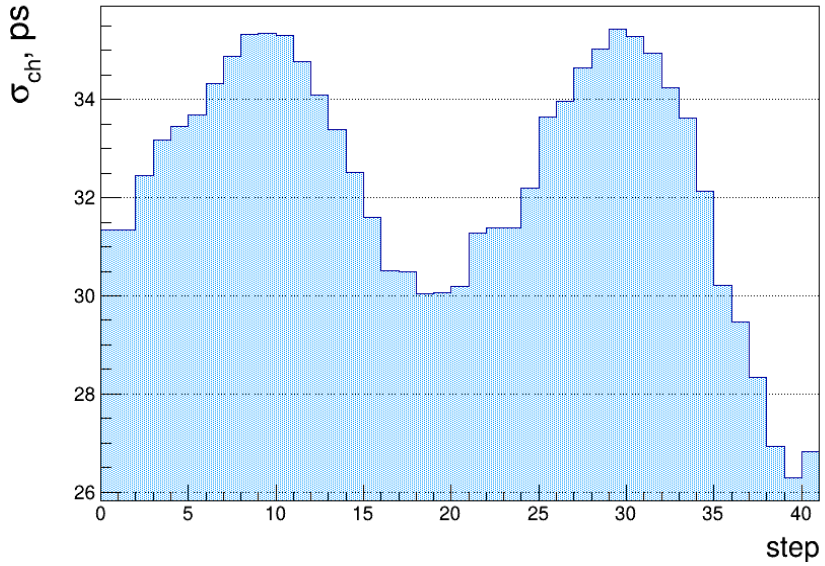


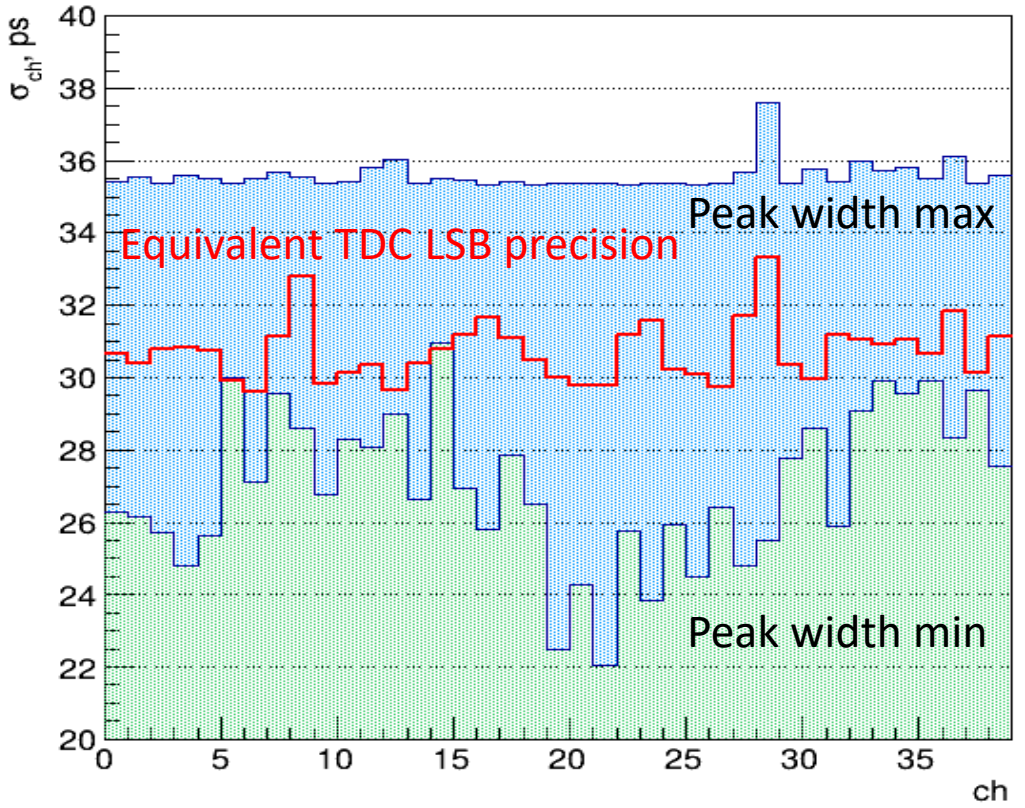
TDC bins width.
(measured with “Code Density Test”)

The TDC single-shot precision

- During the test, pulses with a length in the range of 50.0 .. 50.2 ns were measured with a step of 5 ps.
- For each pulse length the peak width is measured (standard deviation, σ).
- The maximum and minimum of measured peaks width and the equivalent TDC LSB precision are shown. Was used the data generator DG2040 (Cycle-to-Cycle Jitter 5ps).

TDC single-shot precision (ch 0) dependence on the pulse length.
Pulse len = 50ns + step*5ps. The precision depends on the pulse length because of TDC bin width multiplicity.





The equivalent LSB precision:

$$LSB_{EQ} = \sqrt{\frac{N}{T_0 \sum_{i=0}^{i=N-1} BinWidth[i]} \cdot \sum_{i=0}^{i=N-1} BinWidth^3[i]}$$

$$\sigma_{LSB\_EQ} = {}^{LSB_{EQ}}/_{\sqrt{12}}; \begin{cases} BinWidth[\forall i] = 100ps \\ \sigma_{LSB\_EQ} = 29ps \end{cases}; T_0 = 3{,}2ns$$

[4] R Szymanowski et al., "Quantization error in precision time counters," DOI:10.1088/0957-0233/26/7/075002
[5] Stephan Henzler, Theory of TDC Operation, https://doi.org/10.1007/978-90-481-8628-0_3

The developed FPGA based TDC features

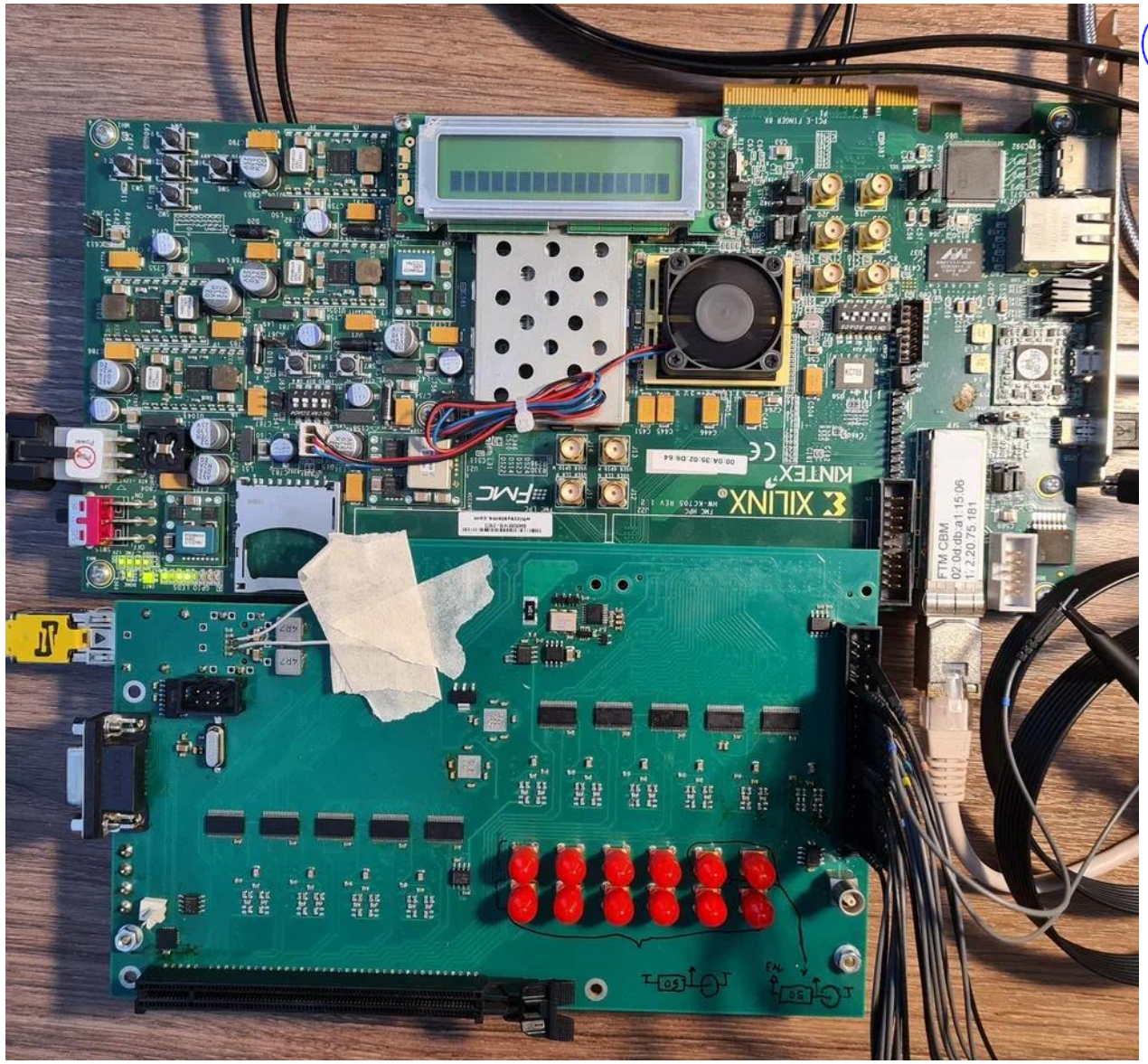
- Kintex 7 FPGA xc7k160: **84 TDC channels / FPGA**
- TDC resolution: **100 ps**
- TDC single-shot precision: **36 ps**
- Excellent TDC linearity
- Low FPGA resource utilization
- Stability of the design is verified using the software suite produced by the FPGA manufacturer

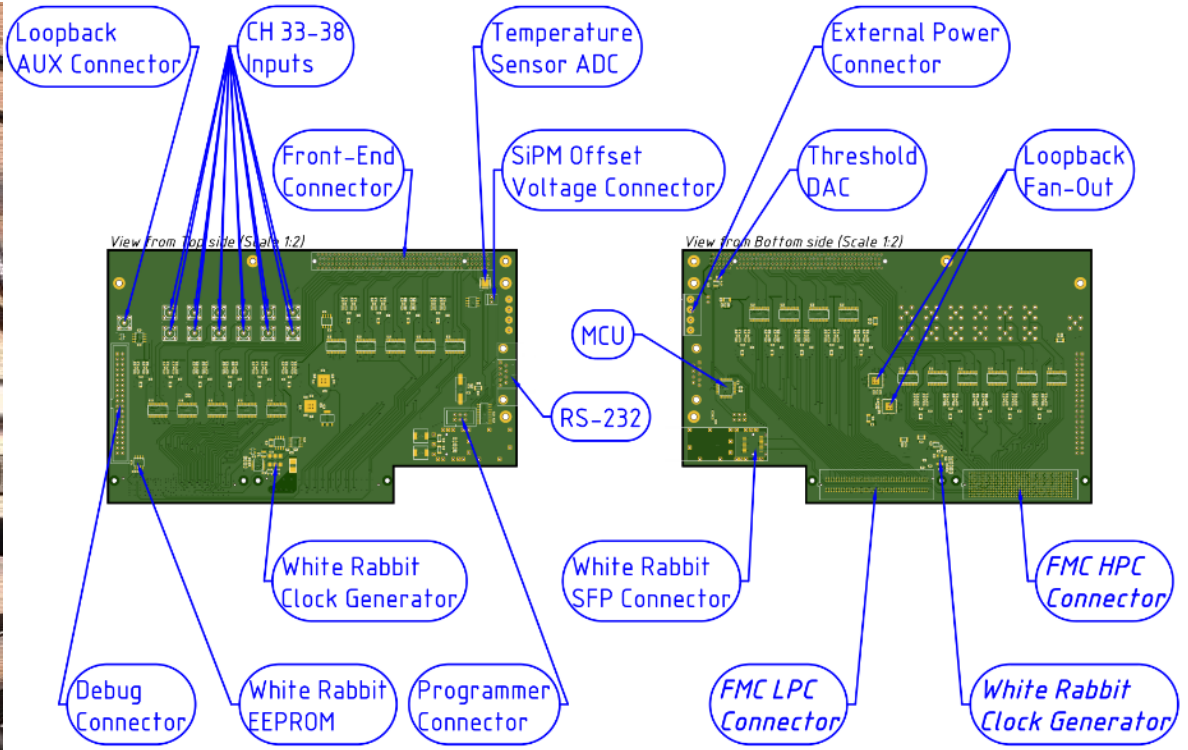
Update:

- Possibly could be improved to 50 ps resolution by decreasing number of channels by two. *R&D needed*.
- Major limitation: IDELAY tap width 39ps.
- Calibration procedure.
- The TDC single shot precision estimation ~22ps

HGND readout v2 prototype (39 channels)

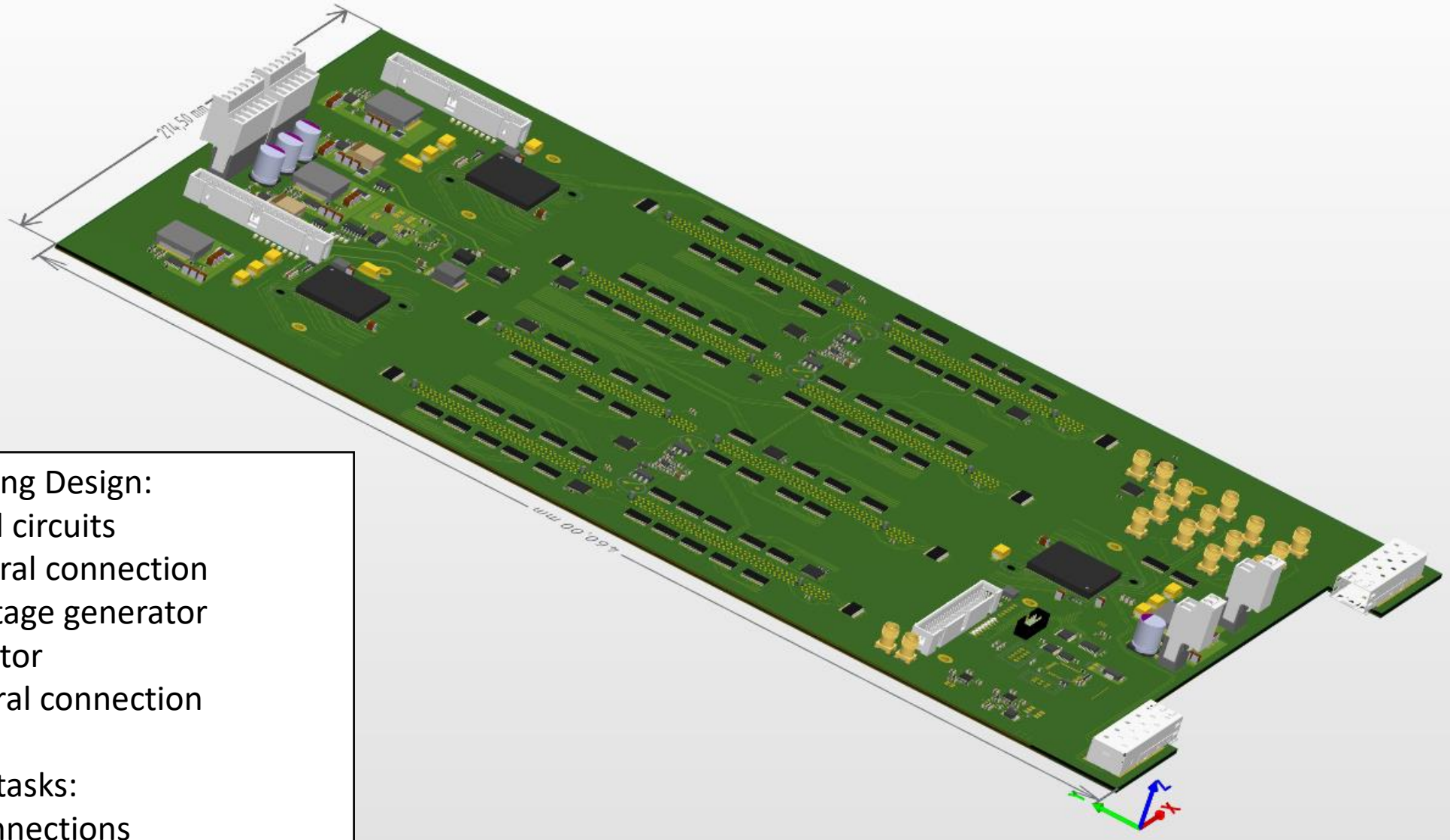
based on the Kintex 7 evaluation board (KC705)





- Addon for Kintex 7 evaluation board
- 33 PCIe + 6 SMA TDC channels
- Ethernet readout
- White Rabbit synchronization
- FPGA loopback for TDC calibration
- Readout board functionality:
  - *PCIe connector for* scintillation matrix*, Temperature sensor, SiPM offset voltage control DAC threshold*

Readout board development

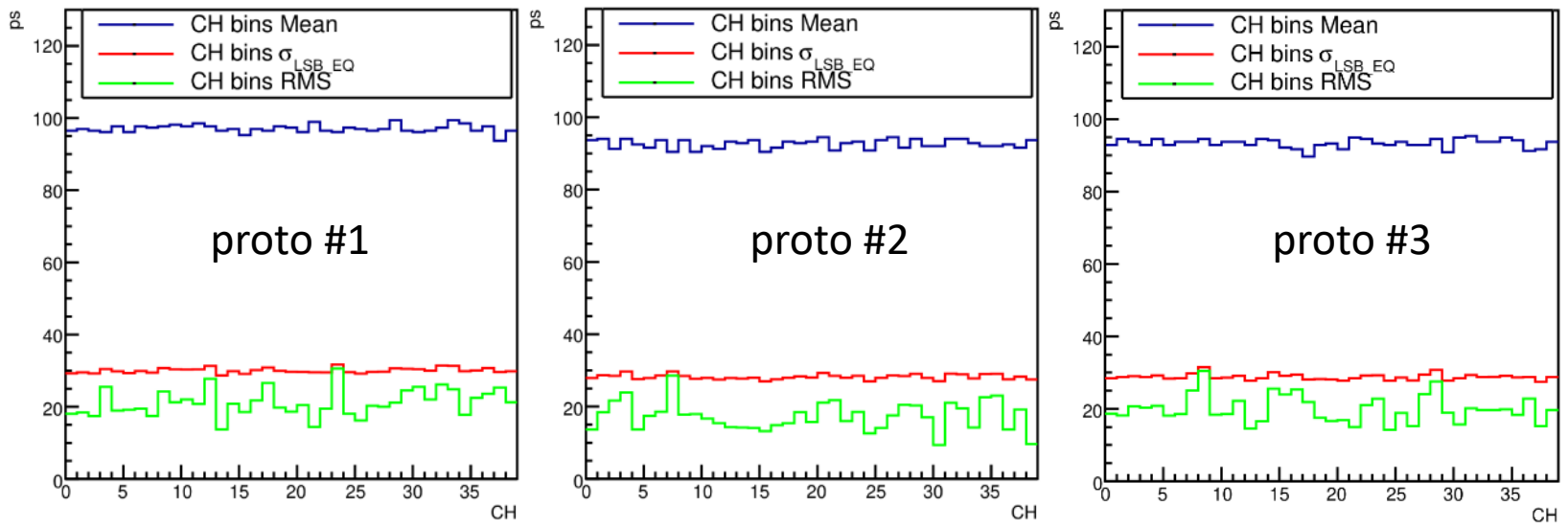


Completed Routing Design:

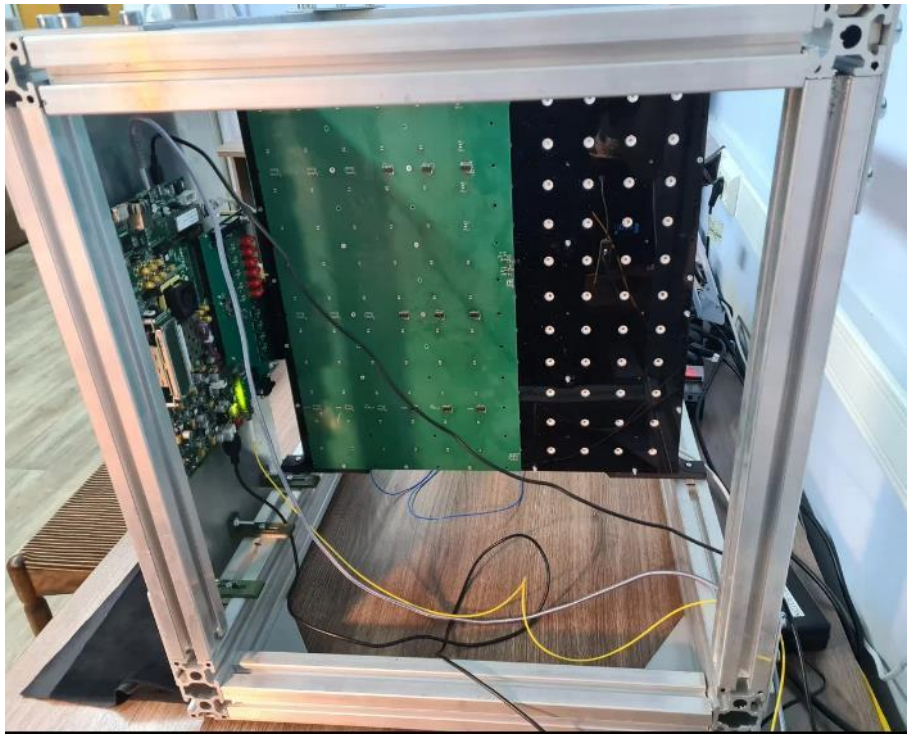
- ✓ Power control circuits
- ✓ FPGA peripheral connection
- ✓ SiPM bias voltage generator
- ✓ Clocks generator
- ✓ MCU peripheral connection

Pending routing tasks:

- ❑ FPGA TDC connections
- ❑ TDC loopback MUX connections



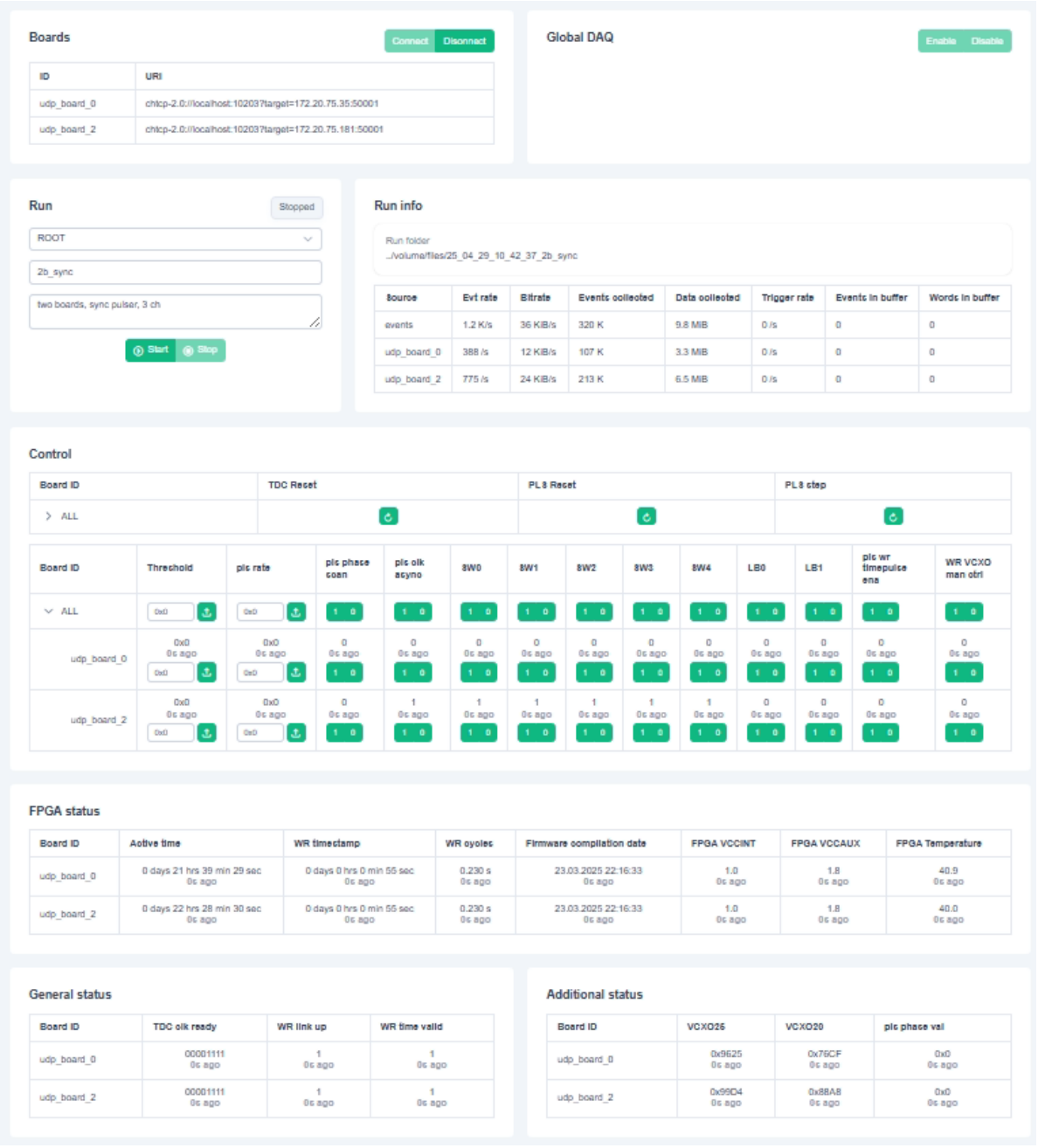
TDC prototype boards timing precision

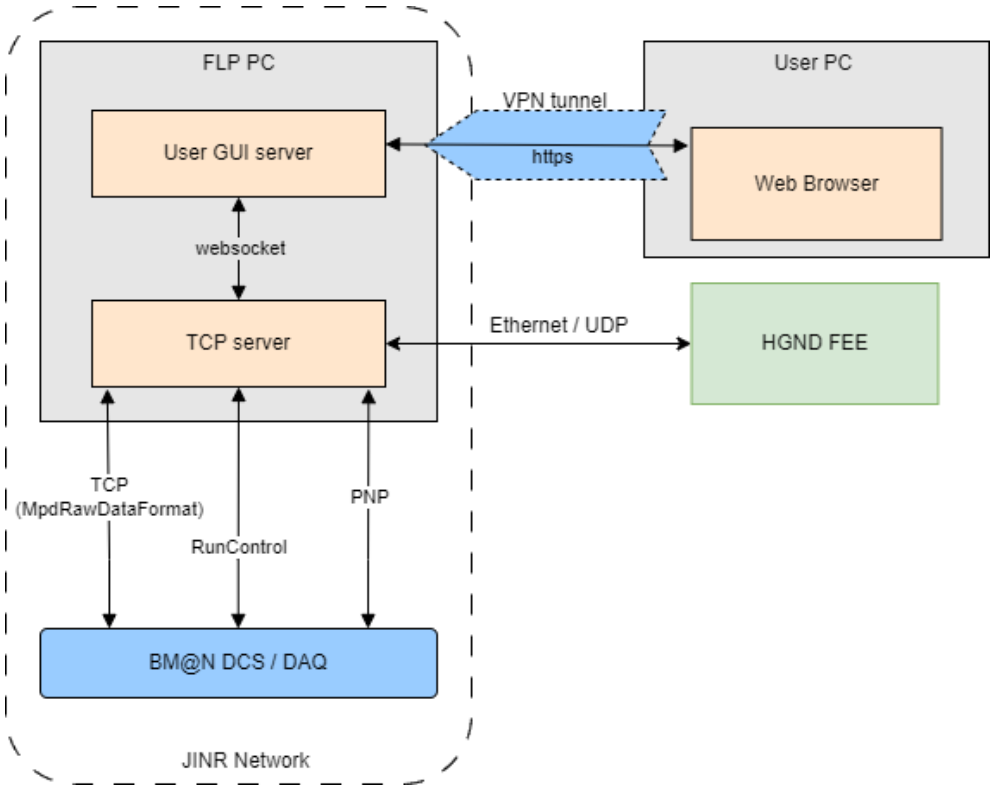


The full functional HGND prototype was assembled.

- Based on readout board proto #1
- ¼ of matrix SiPM & LED channels
- Ethernet readout
- White Rabbit synchronization
- PCIe connector for scintillation matrix
- Temperature sensor
- SiPM threshold DAC control
- Match HGND geometry

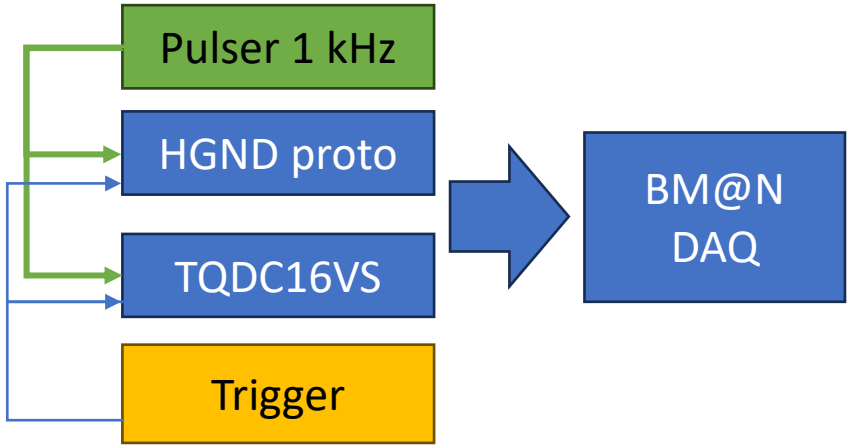
Server development status and preparation for integration into BM@N



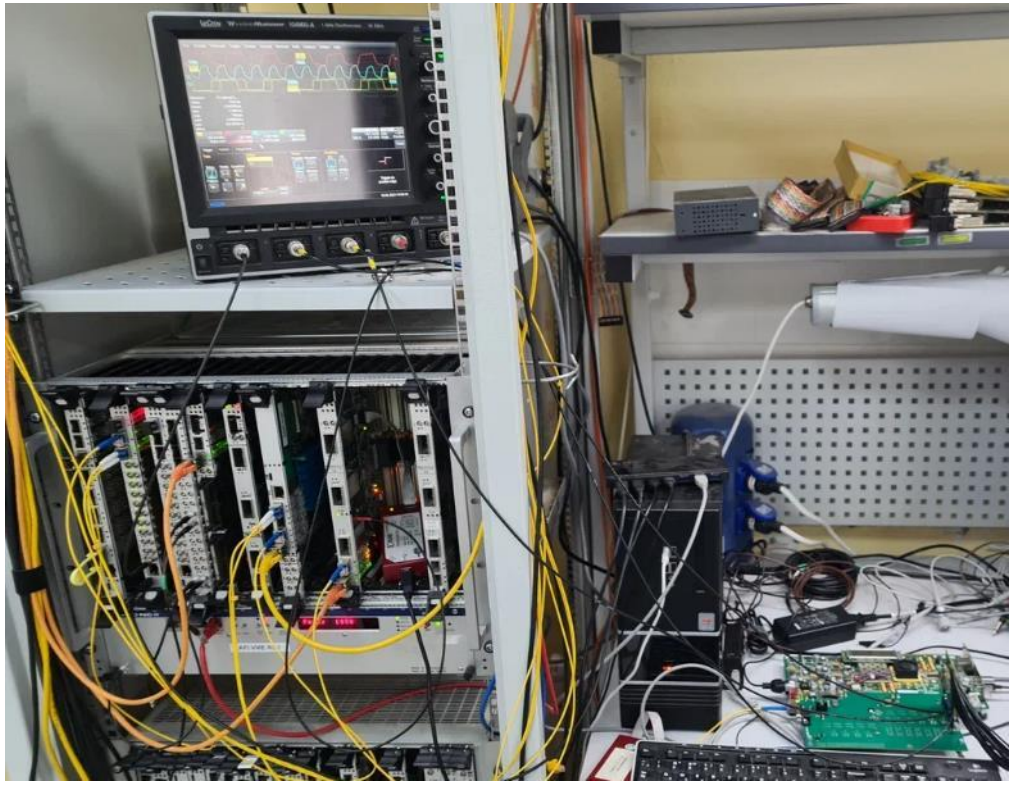


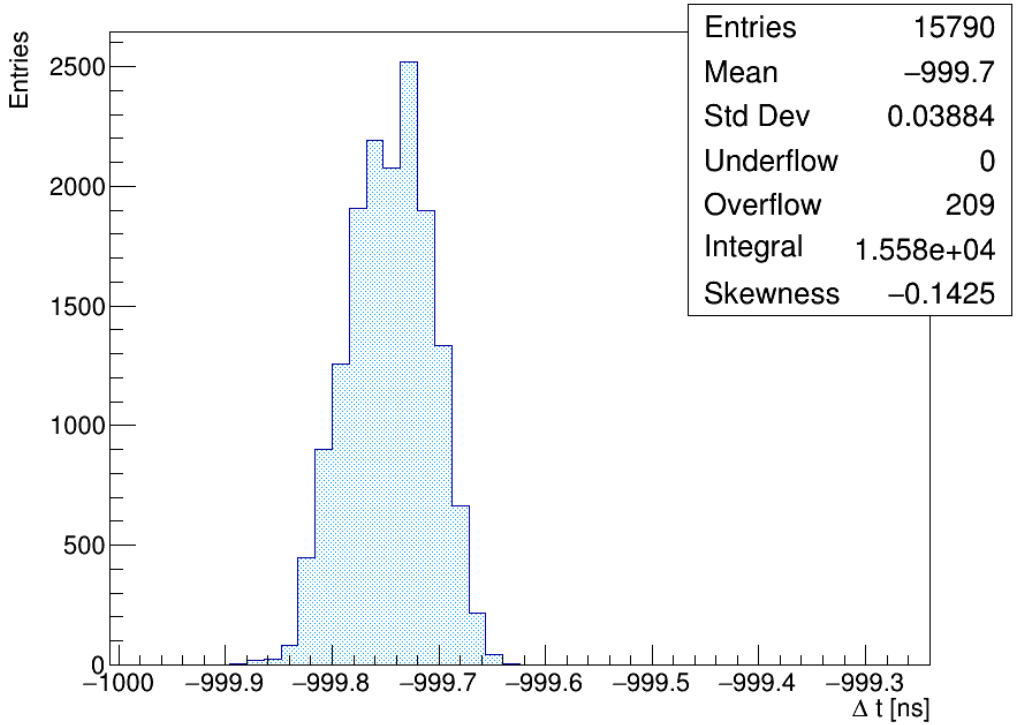
- Web interface: status & configuration
- Global DAQ + DCS
- Standalone data acquisition
- BM@N integration to be tested
- Crucial facilities was tested
- Working on minor tasks

The HGND integration tests



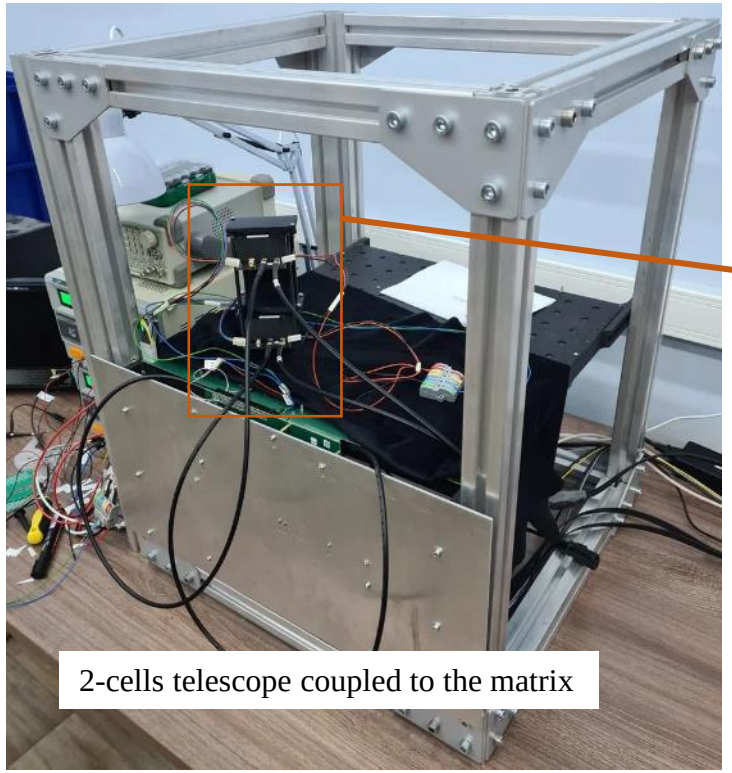
- The HGND readout prototype was connected to BM@N DAQ.
- Synchronous pulse was propagated to HGND and TQDC board.
- BM@N DAQ event builder and run control software used.
  - ✓ Continuous readout
  - ✓ Time synchronization (σ = 39 ps)
  - ❑ Triggered readout
  - ❑ Experiment DAQ control

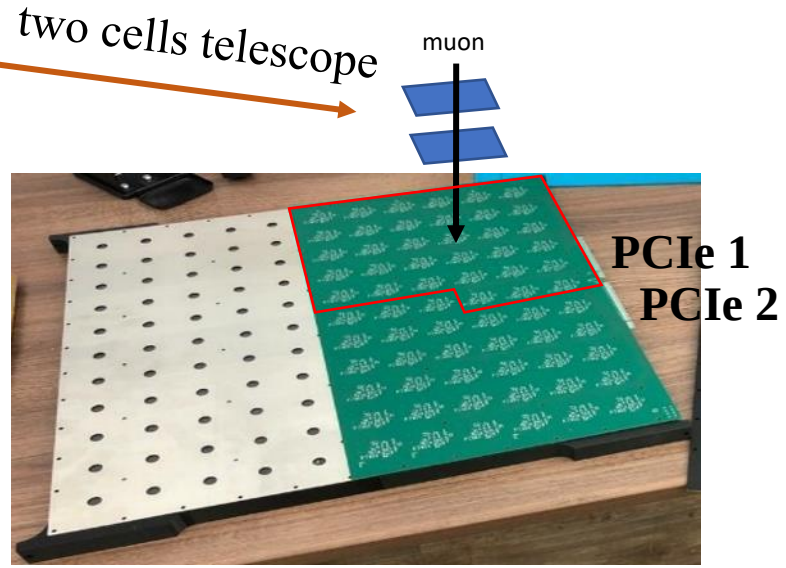




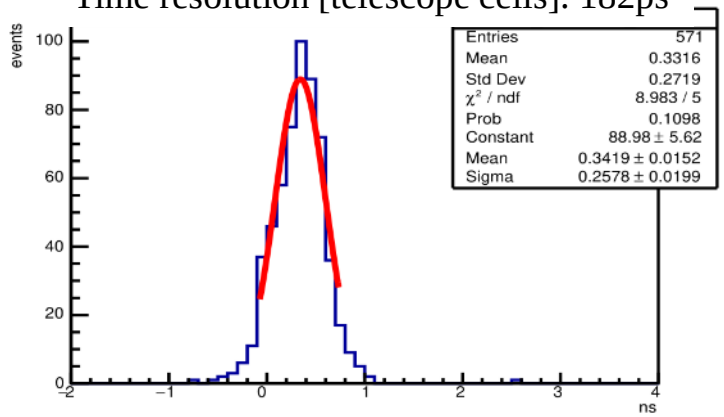
Time synchronization HGND – TQDC board

The HGND prototype tests with cosmic muons

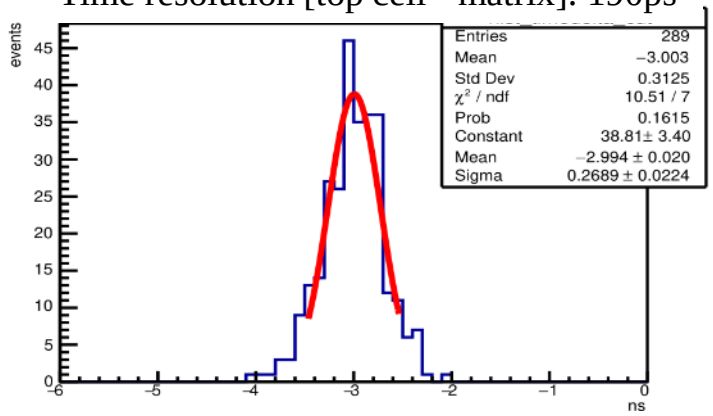




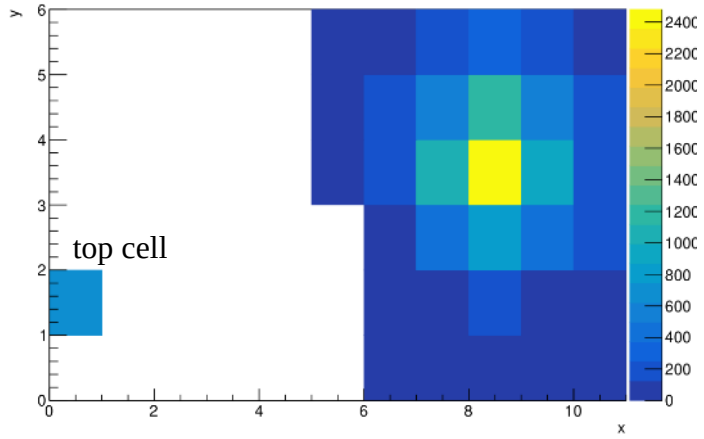
Time resolution [telescope cells]: 182ps



Time resolution [top cell - matrix]: 190ps



The time correlated events: bottom cell – matrix



Cosmic runs was collected in two configuration:

- Normal position (like placement on the BM@N)
- Horizontal position with 2 cells telescope

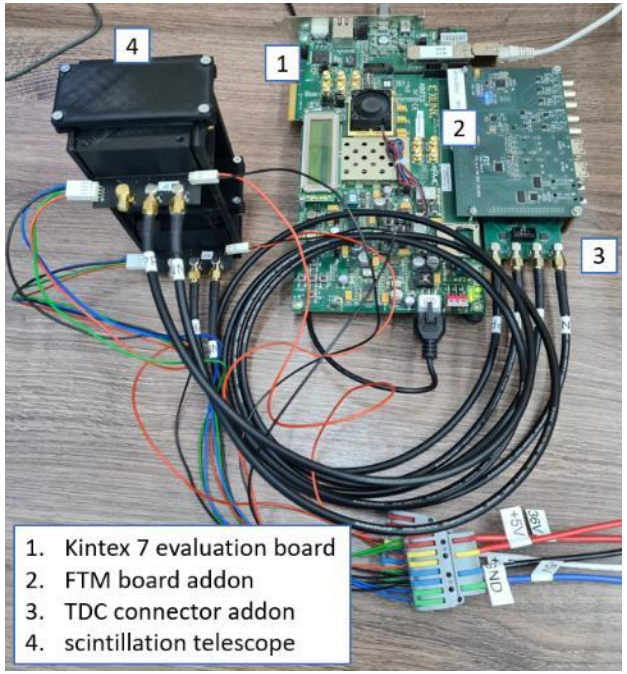
✓ Results shows the same time resolution between telescope connected via SMA and matrix connected via PCIe: 182 and 190 ps per channel.

➢ Testing all functionality: readout, LED calibration, temperature sensor, geometry, light-isolating

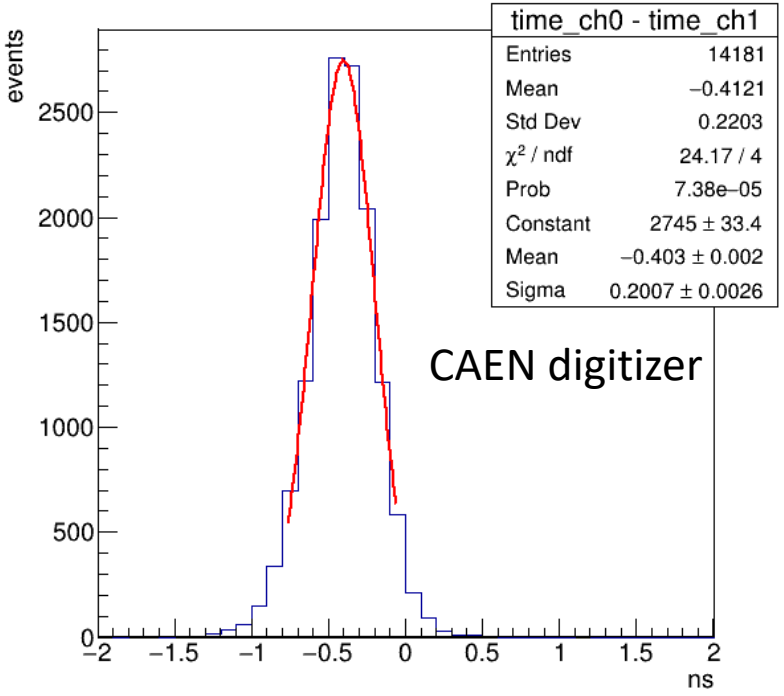
➢ FEE Mass-production

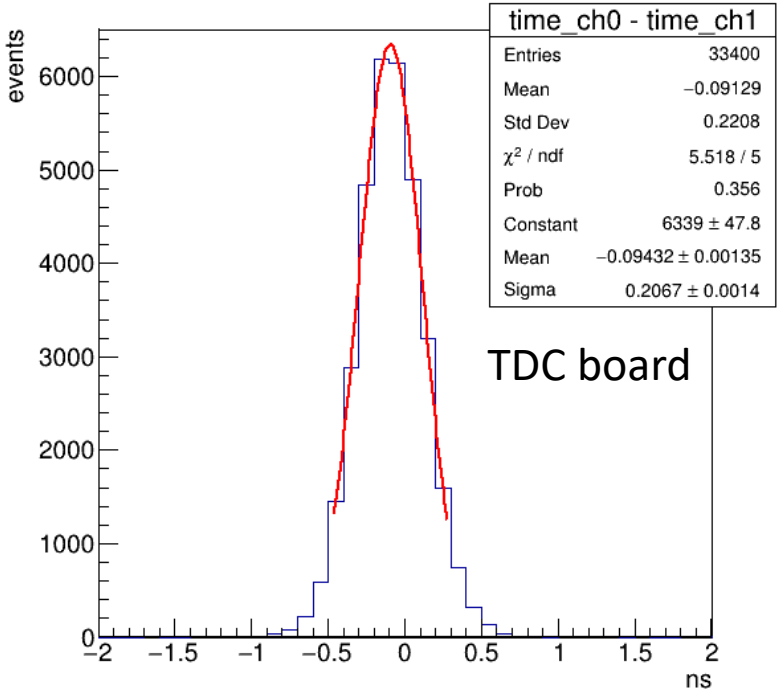
The FPGA TDC test results

The time resolution measurements with the FPGA TDC prototype board were performed with the 280 MeV electron beam on the “Pakhra” synchrotron in LPI (Moscow, Russia).



HGND scintillator cells telescope is connected to 2-channels TDC prototype based on KC705 evaluation board





The time difference distributions of two cells of the telescope measured with the CAEN digitizer (left) and the FPGA TDC prototype board (right). Time resolution is ***146 ps*** per single HGND channel.

Conclusions

- The new High Granular neutron Detector is under construction
  - New EQR MPPC
  - 2000 channels without cables
  - FPGA based TDC SSP 36 ps

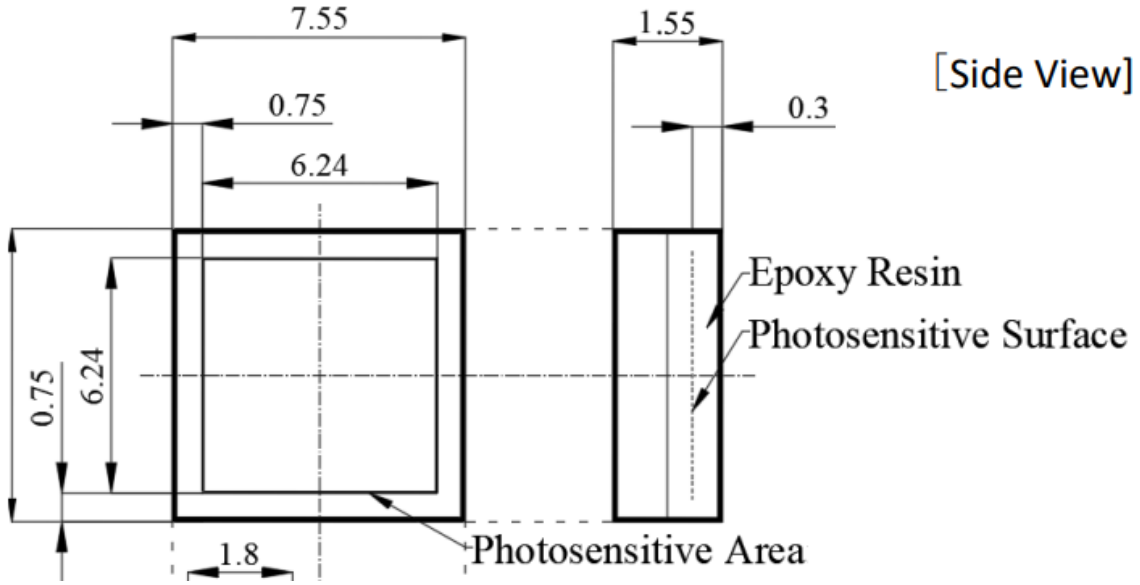
- Mechanical part was assembled
- Working on routing readout board
- Integration tests into BM@N DAQ are ongoing

Thank you for your attention!

BACKUP

Type	EQR15 11-1010D-S	EQR15 11-3030D-S	EQR15 11-6060D-S	EQR15 22-1313D-S
Effective Pitch	15 μm			
Element Number	1×1			2×2
Active Area	1.0×1.0 mm²	3.0×3.0 mm²	6.24×6.24 mm²	1.3×1.3 mm²
Micro-cell Number	4444 /mm²			
Typical Breakdown Voltage (V_B)	30 V			
Temperature Coefficient for V_B	28 mV/℃			
Recommended Operation Voltage	V_B + 8 V			
Peak PDE @ 420nm	45 %			
Gain	4.0 × 10⁵			
Dark Count Rate（DCR）	250 kHz / mm²			
Terminal Capacitance	5.6 pF / mm²			

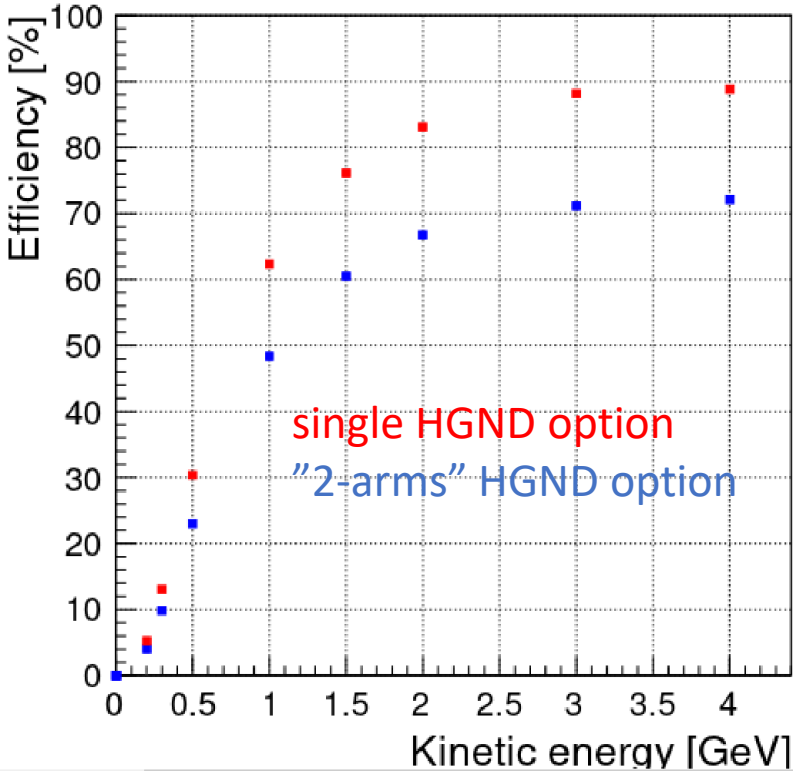
: parameters are measured at their recommended operation voltage and 20 ℃， and they can operate at 77 K.

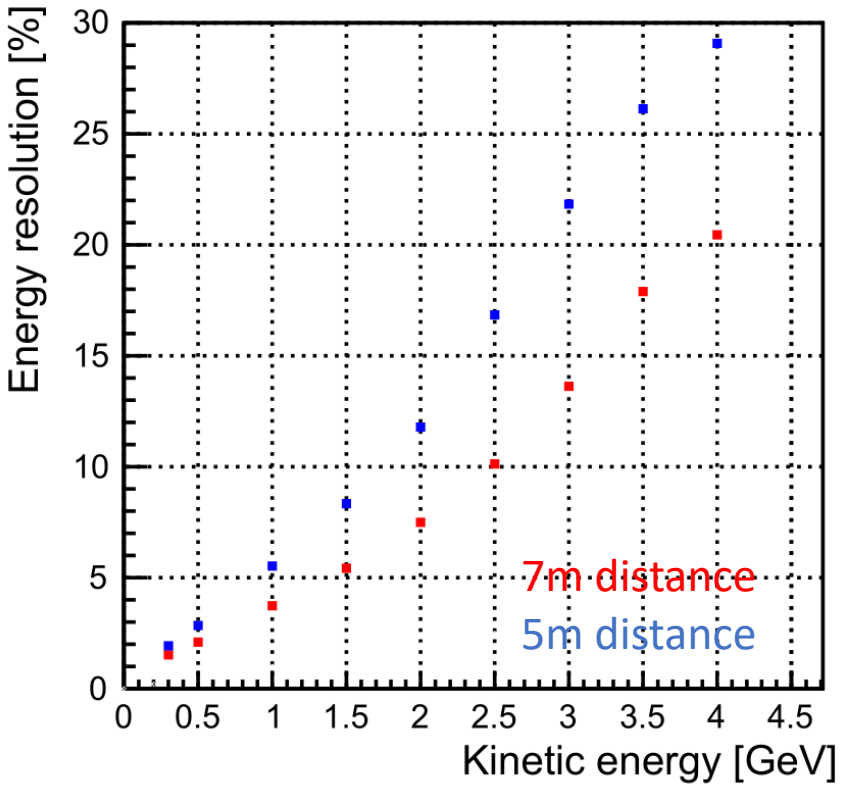


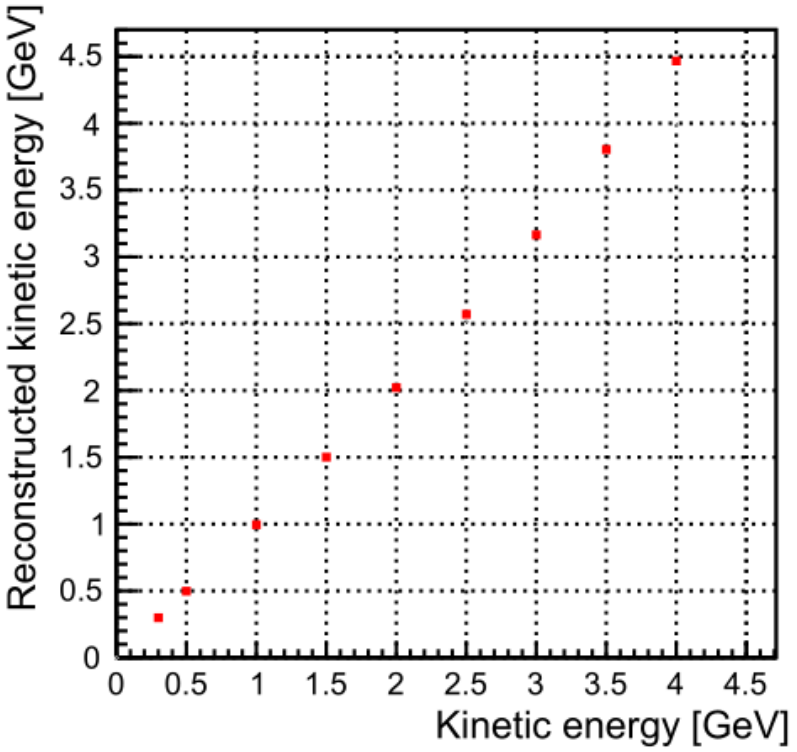
- conversion factor of 1.8 mV/phe
- MIP light output value of 158±9 phe

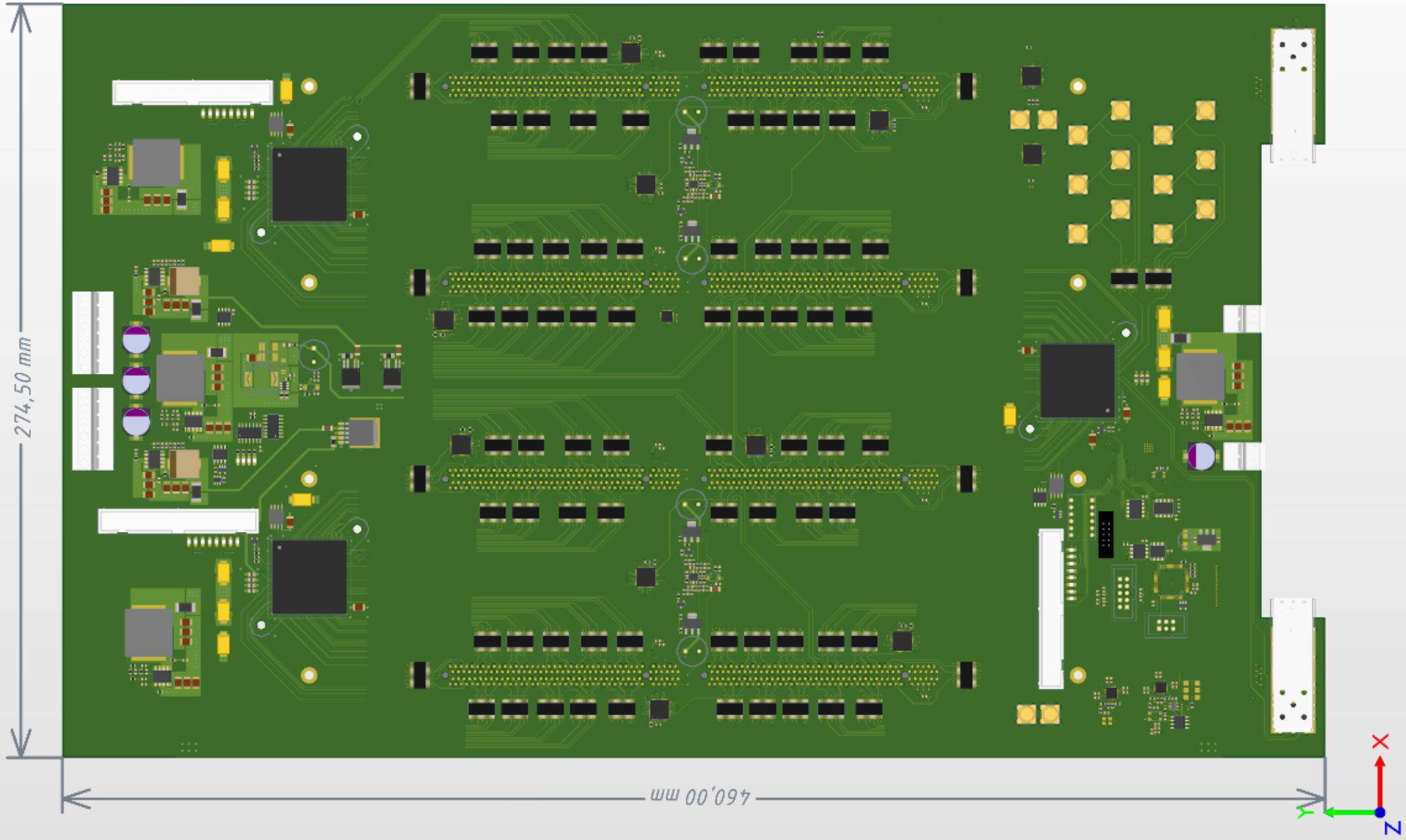
- preamplifier LMH6629MF op-amp (with a gain of 20 dB and a bandwidth of 600 MHz at a 3 dB level, and noise of <2.2 nV/√Hz).

In such SiPMs, the quenching resistance is integrated within the epitaxial layer, increasing the density of cells. Reduced junction capacitance combined with a relatively low quenching resistance, leads to a fast recovery time. Additionally, the high geometric fill factor of these SiPMs allows for a wide dynamic range with high photon detection efficiency (PDE).


Efficiency [%]
Kinetic energy [GeV]
single HGND option
”2-arms” HGND option

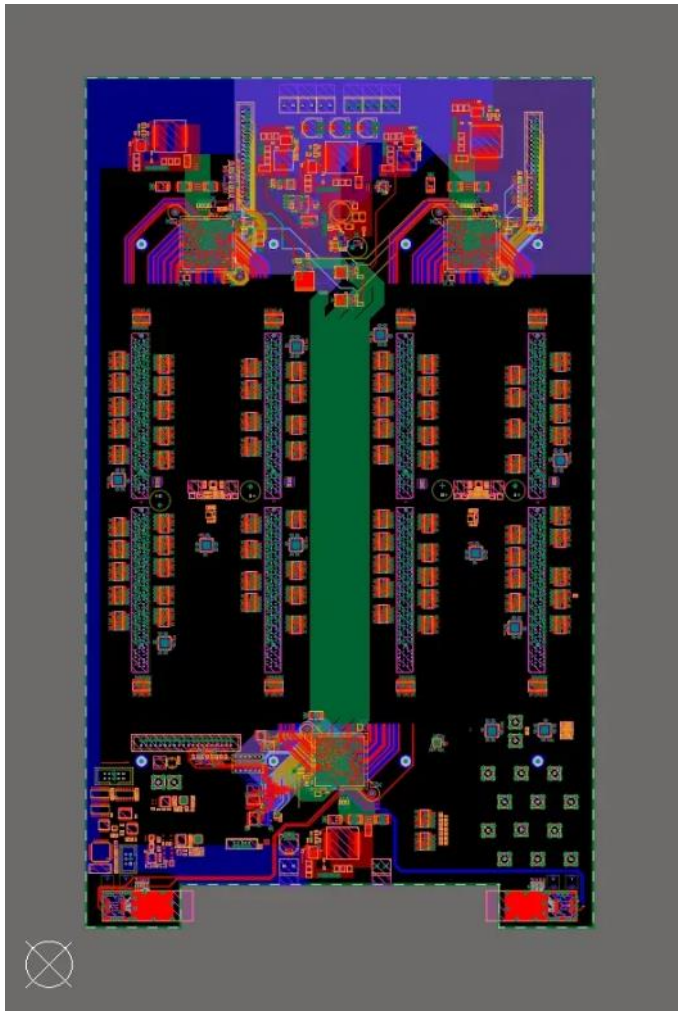

Energy resolution [%]
Kinetic energy [GeV]
7m distance
5m distance


Reconstructed kinetic energy [GeV]
Kinetic energy [GeV]

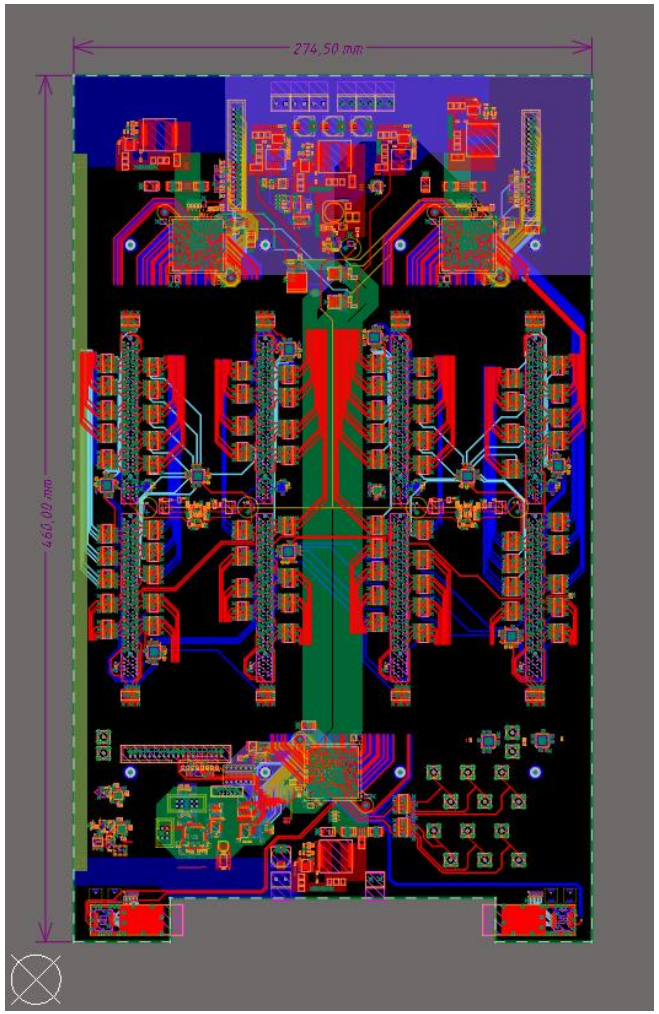

274,50 mm
460,00 mm
X
Y
Z

Status of the HW development

Readout board routing status ***May 25***



Readout board routing status ***June 25***



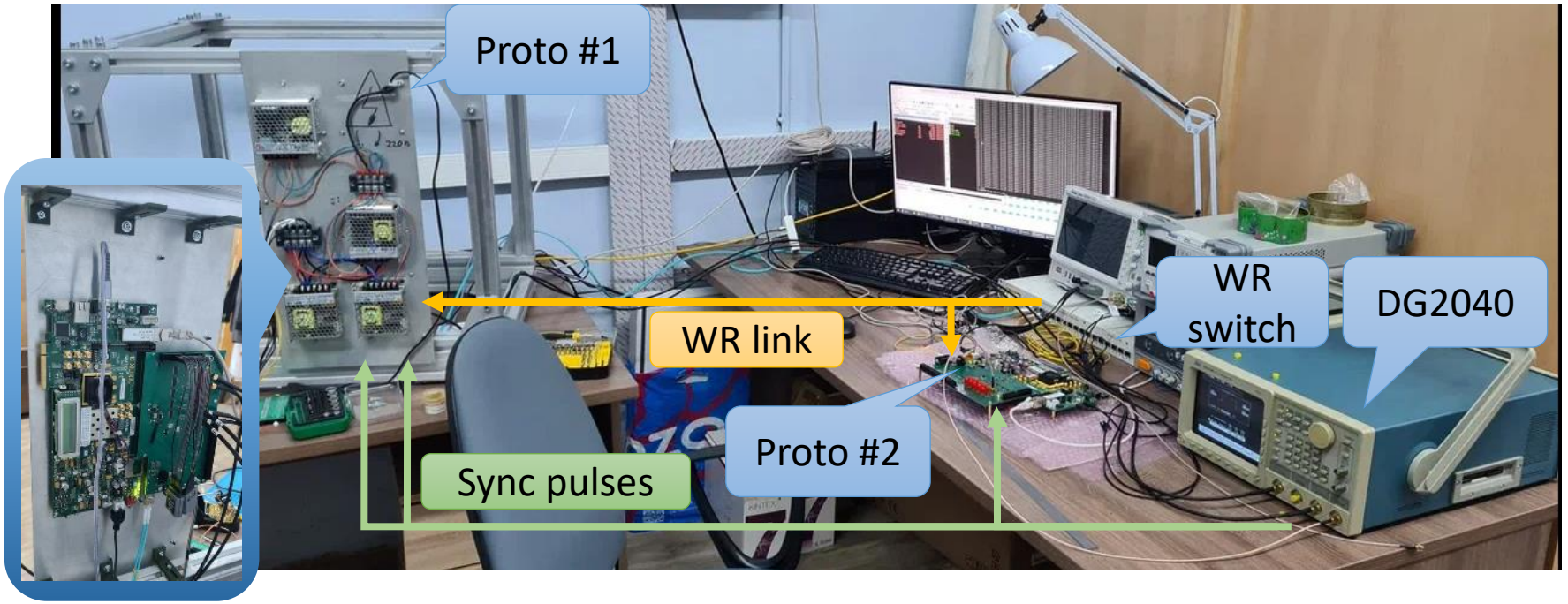
Completed Routing Design:

- ✓ Power control circuits
- ✓ FPGA peripheral connection
- ✓ SiPM bias voltage generator
- ❑ Clocks generator
- ❑ MCU peripheral connection

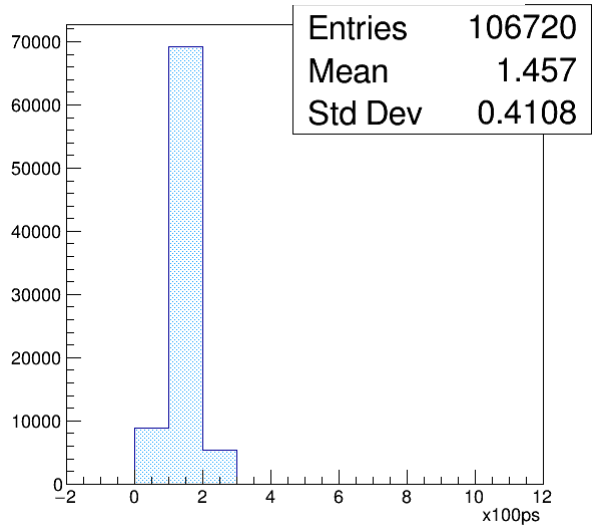
Pending routing tasks:

- ❑ FPGA TDC connections
- ❑ TDC loopback MUX connections

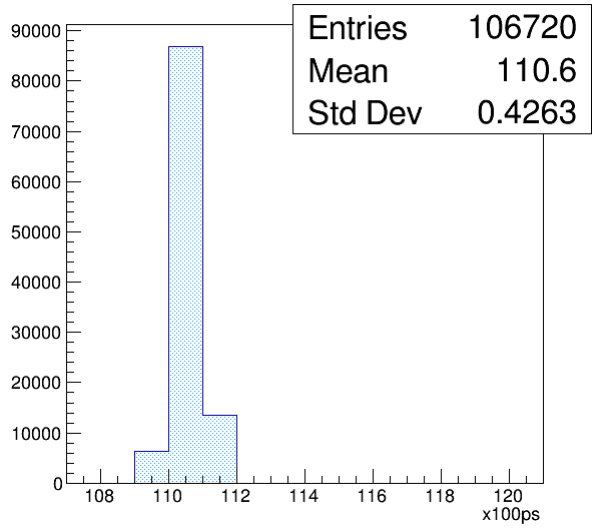
WR cross board synchronization test



Two channels on proto #1



proto #1 – proto #2



- Two prototype readout boards are synchronized using a White Rabbit switch.
  - Proto #1 receives pulses from two channels.
  - Proto #2 receives pulses from a single channel.
- The intrinsic jitter of the **DG2040** generator is **5 ps**.
- The TDC channel's time resolution is **30 ps**.
- The time difference distributions (both cross-board and single-board) is **42 ps** and match the TDC's resolution.

FPGA TDC and calibration pulser clocks layout