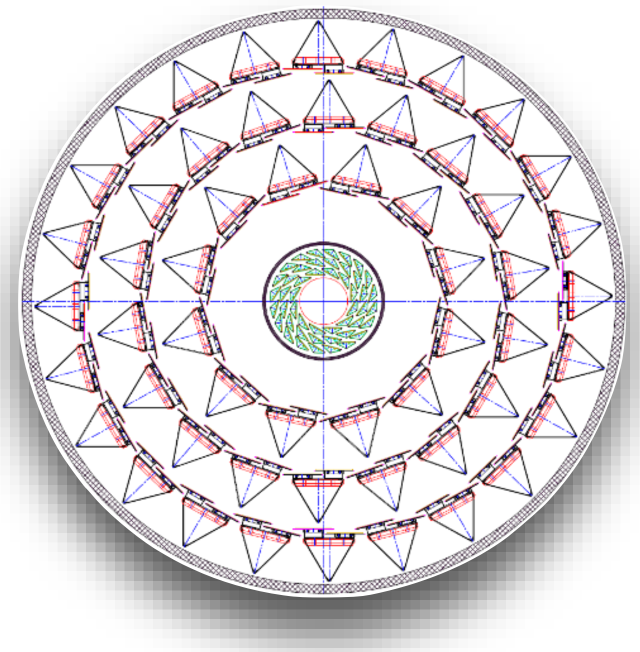


MPD ITS current status

Ekaterina Tsapulina LHEP-JINR for the MPD-ITS

LXXV NUCLEUS 2025,

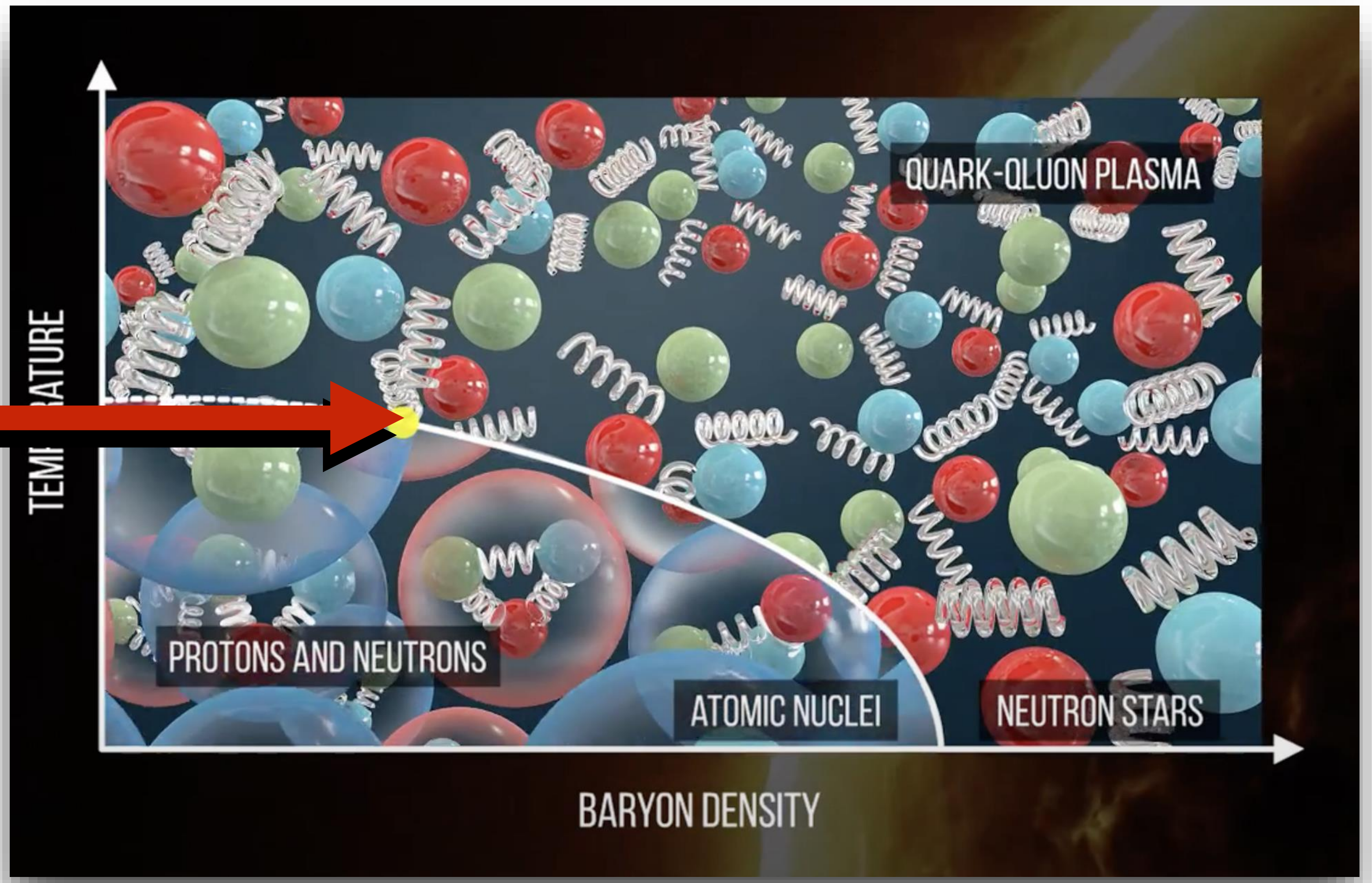
St.-Petersburg, 1-6 July 2025

Outline

- Introduction.
- Physical motivation of using vertex detectors.
- Status of:
  - The MPD ITS layout with description of its basic components.
  - Computer simulations of MPD ITS for D-mesons identification.
  - ITS mechanics.
  - MICA chip and R@D effort at CCNU (Wuhan).
  - RU and PU R@D at USTC (Hefei).
  - Assembly site.
  - Leakless water & dry gas cooling systems.
- Conclusions and outlook

The NICA collider @ JINR.

Nuclotron-based Ion Collider fAcility



$$\mathrm{A+A}\ @\ \sqrt{s_{NN}} = 4 - 11 GeV$$

QGP probes

p(uud) n(ddu)

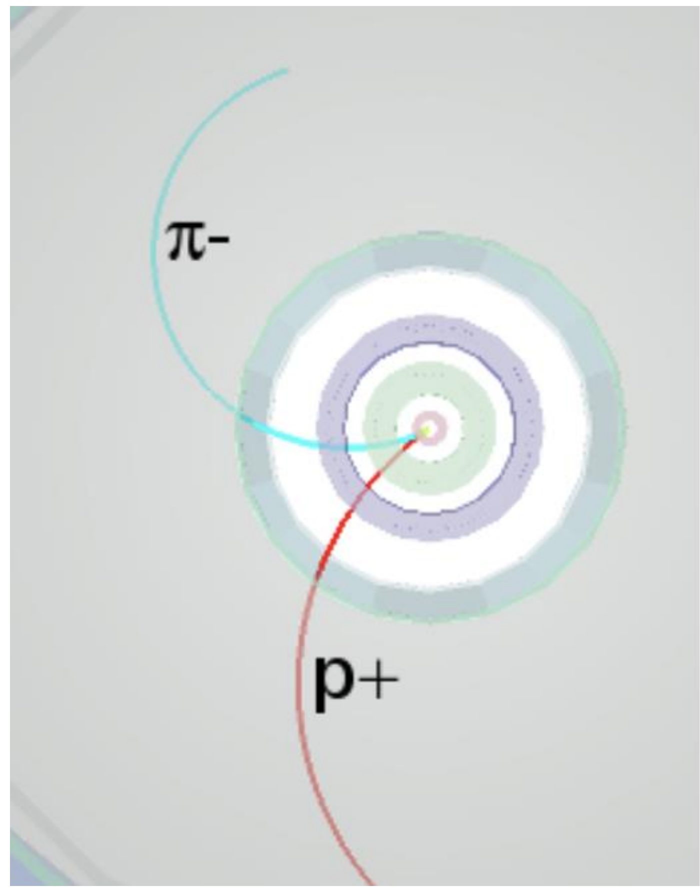
$\Lambda(uds)$ $\Xi^-(dss)$ $\Omega^-(sss)$

$D^+(c\bar{d})$ $D^0(c\bar{u})$

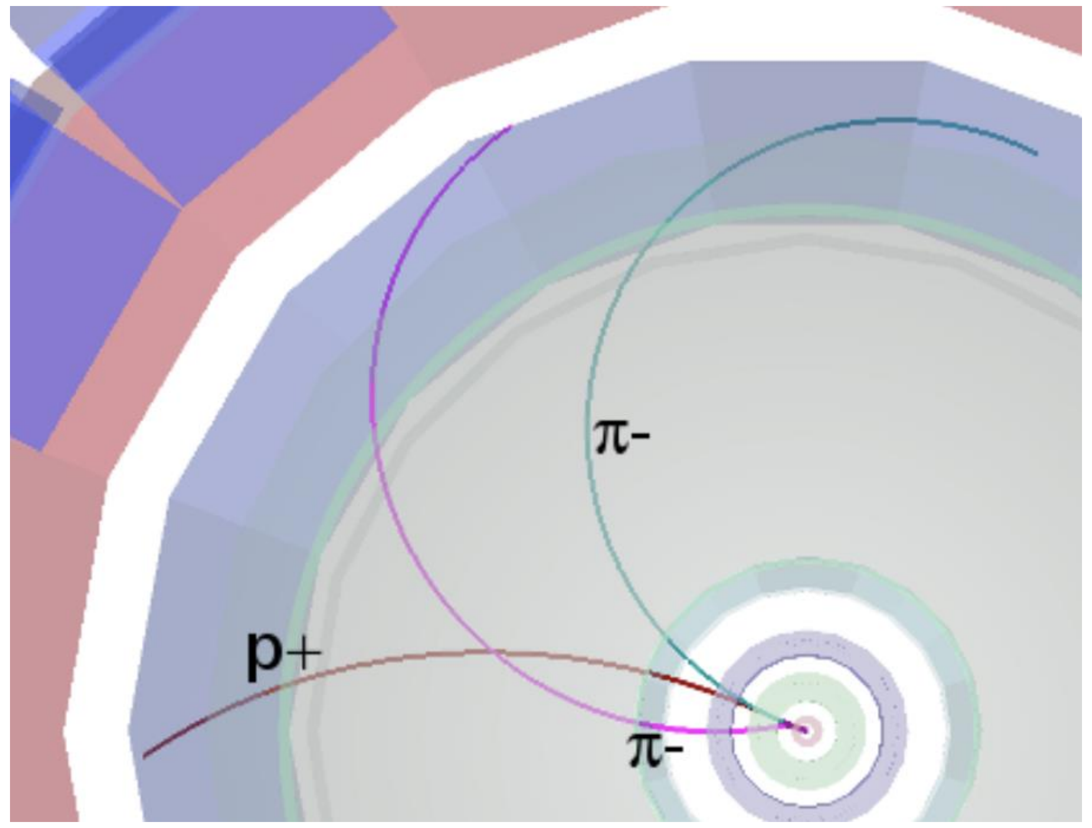
Hadron	Mass (MeV/cm²)	Average path length $c\tau$(mm)	Decay channel	BR (%)
Λ	1115.68 ± 0.01	78.9	$\pi^- + \mathrm{p}$	63.9
Ξ^-	1321.71 ± 0.07	49.1	$\pi^- + \Lambda^0$	99.9
Ω^-	1672.45 ± 0.29	24.6	$K^- + \Lambda^0$	67.8
D^+	1869.62 ± 0.20	0.312	$\pi^+ + \pi^+ + K^-$	9.13
D^0	1864.84 ± 0.17	0.123	$\pi^+ + K^-$	3.89

Strong Magnetic Field

(Decay Topology)

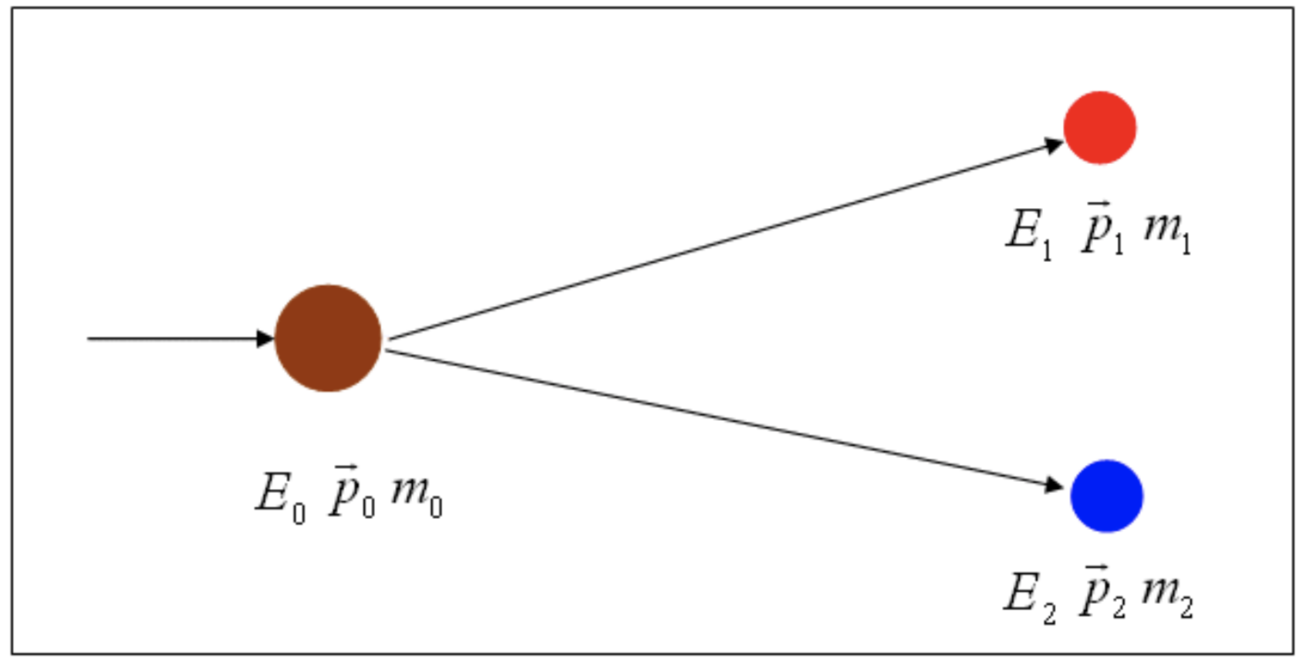


$\Lambda \rightarrow p + \pi^-$



$\Xi^- \rightarrow \pi^- + \Lambda \rightarrow \pi^- p + \pi^-$

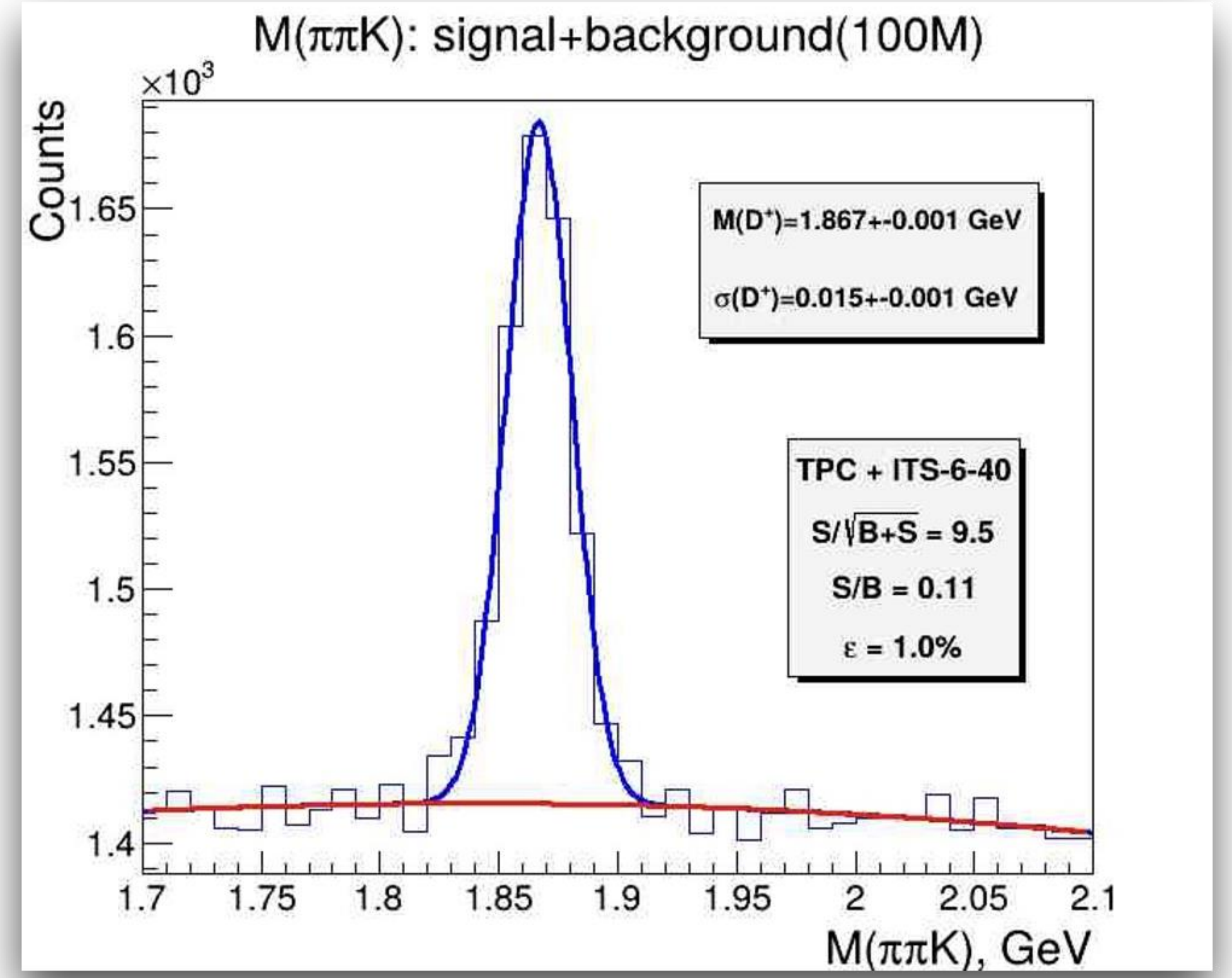
(Invariant Mass Spectrum)



$$m_0 = \sqrt{m_1^2 + m_2^2 + 2(E_1 E_2 - \vec{p}_1 \vec{p}_2)}$$

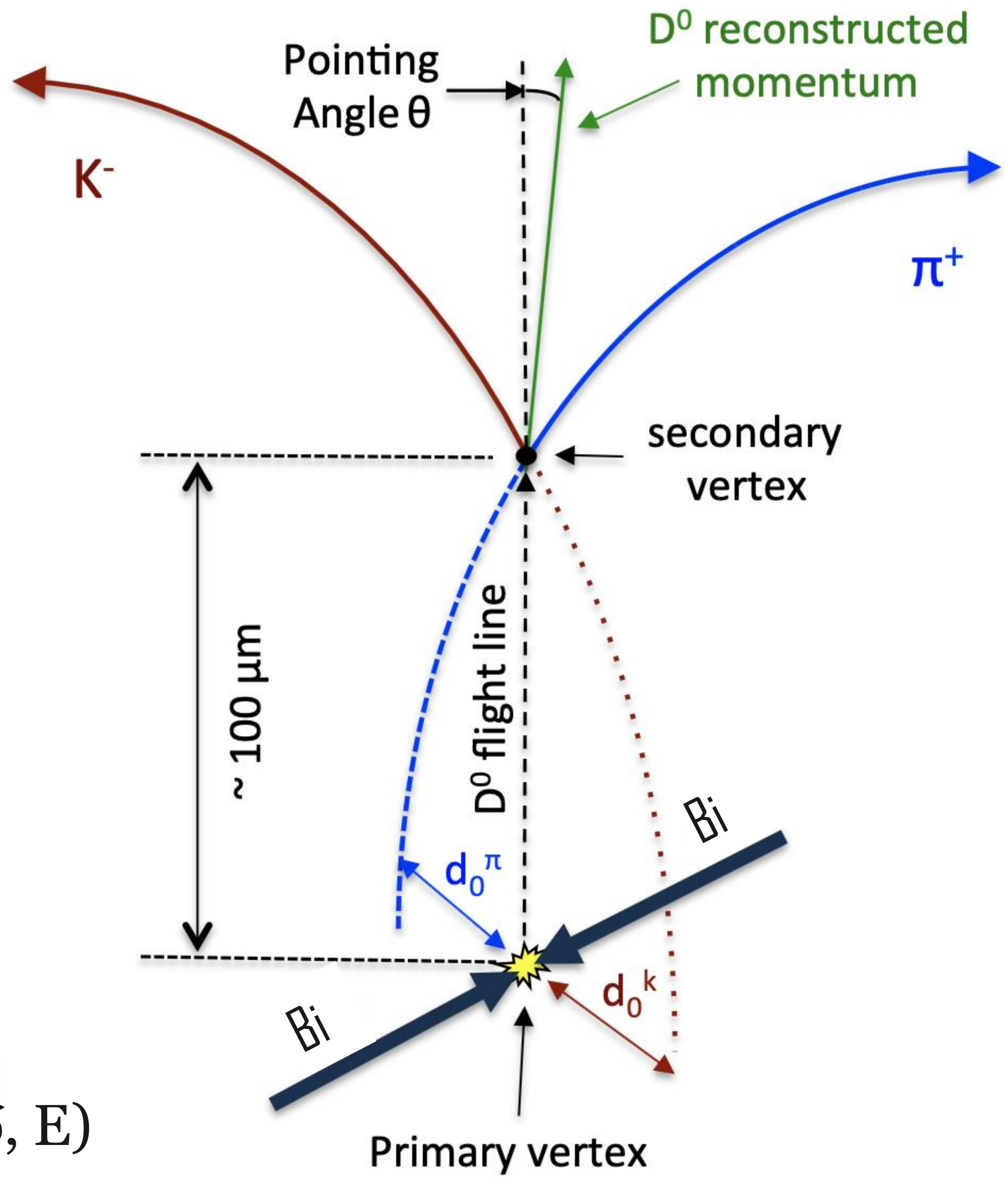
Physical motivation of using vertex detectors

Like finding a needle in a haystack



Signal + Background

(m, $\vec{p}$, E)



High resolution is needed! (Continuous upgrade of the system)

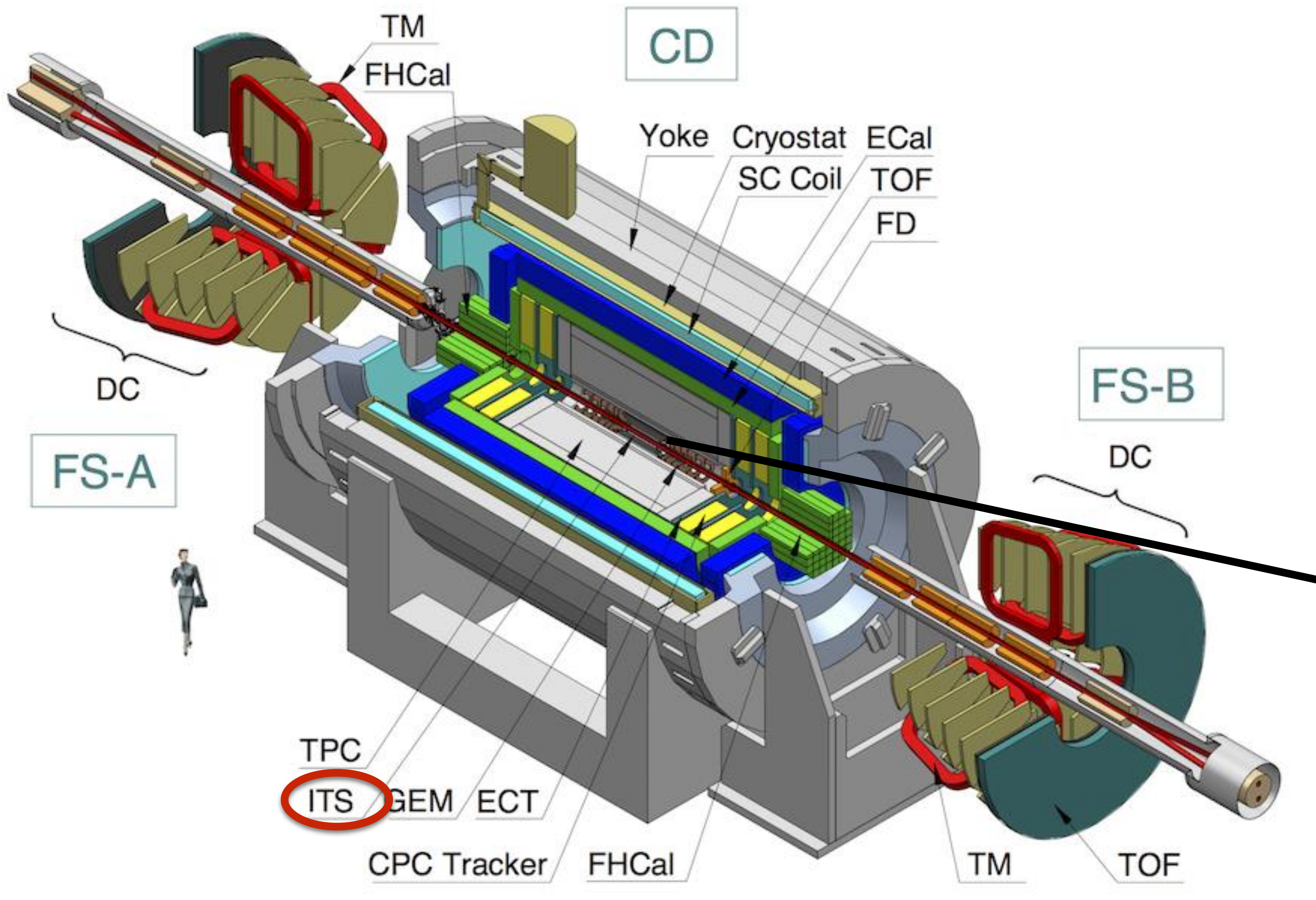
The MPD ITS layout with description of its basic components

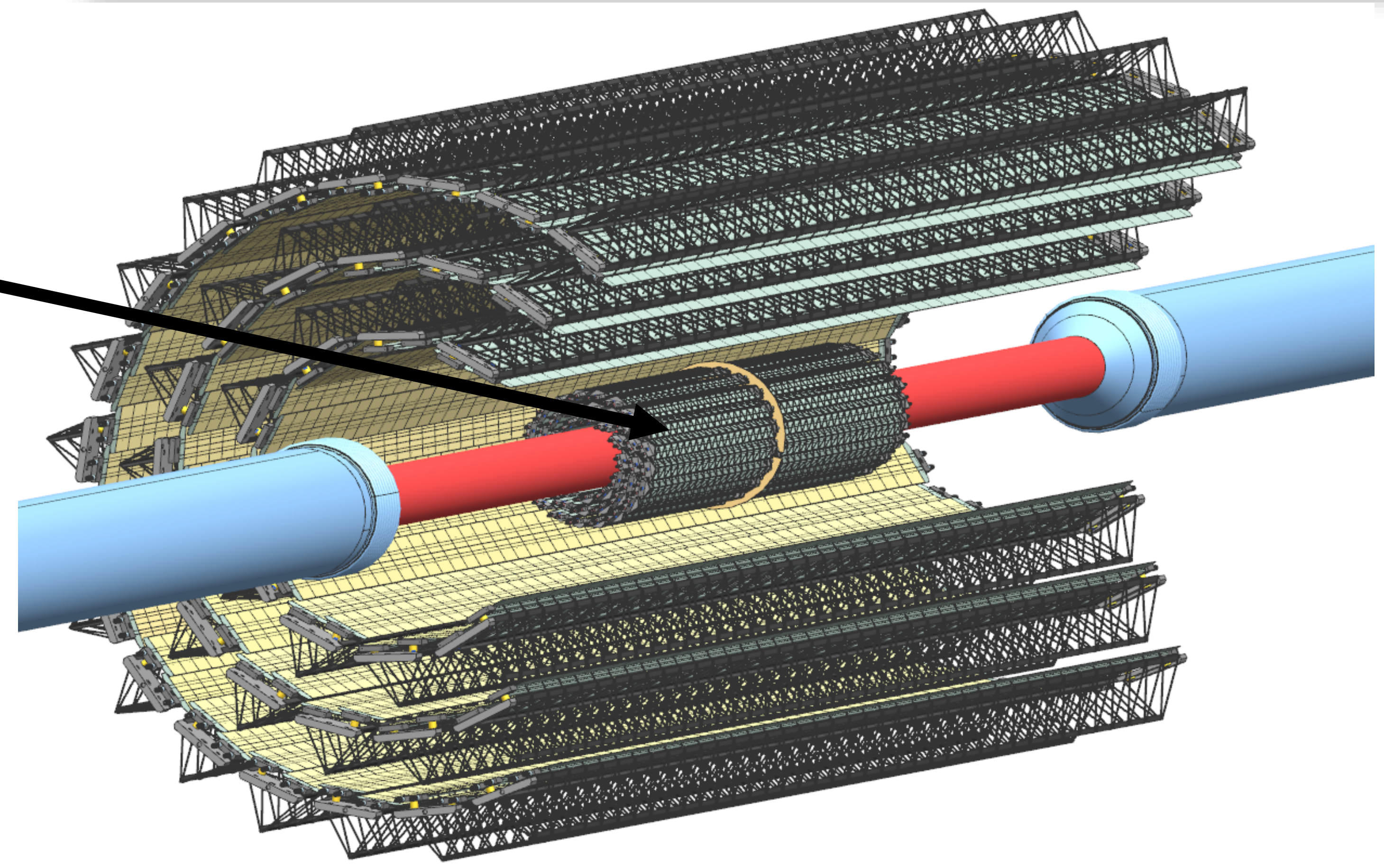
<u>MPD-ITS structure:</u> 3-layers Inner Barrel + 3-layers Outer Barrel .

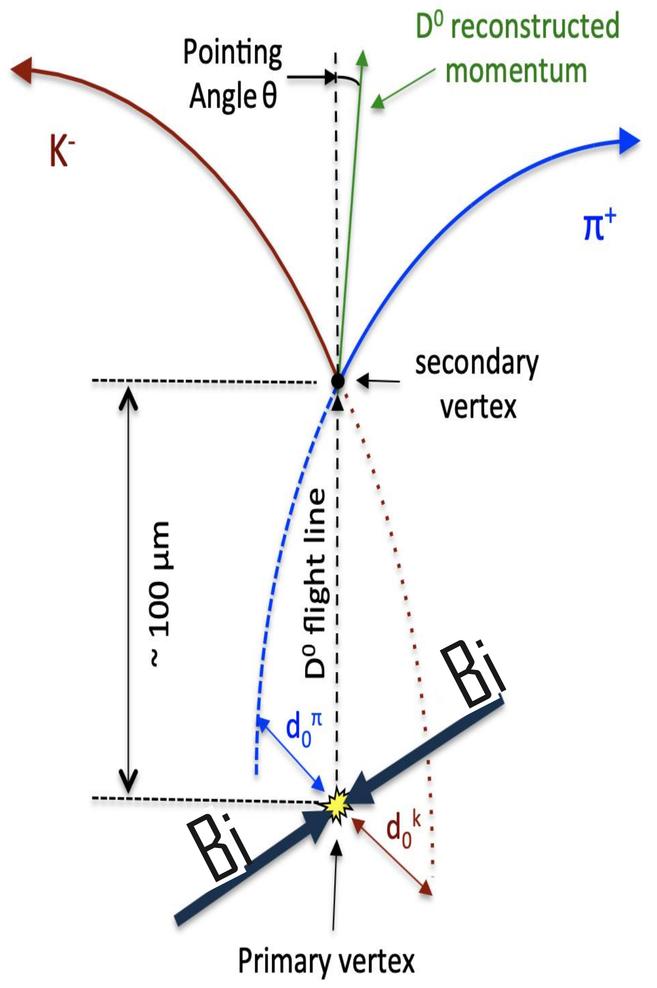
It will supplement the TPC for the precise tracking, momentum determination and vertex reconstruction for **low Pt momenta hyperons** (Λ, Ξ, Ω) and identification of **D-mesons.**

<u>Some of the MPD-ITS requirements:</u>

- **Fast, high granularity CMOS pixel sensors with low noise level.**
- **Spatial resolution of track coordinate registration at the level of ~5–10 μm.**
- **Material budget as low as possible.**
- **Positioned as close as possible to the interaction diamond**



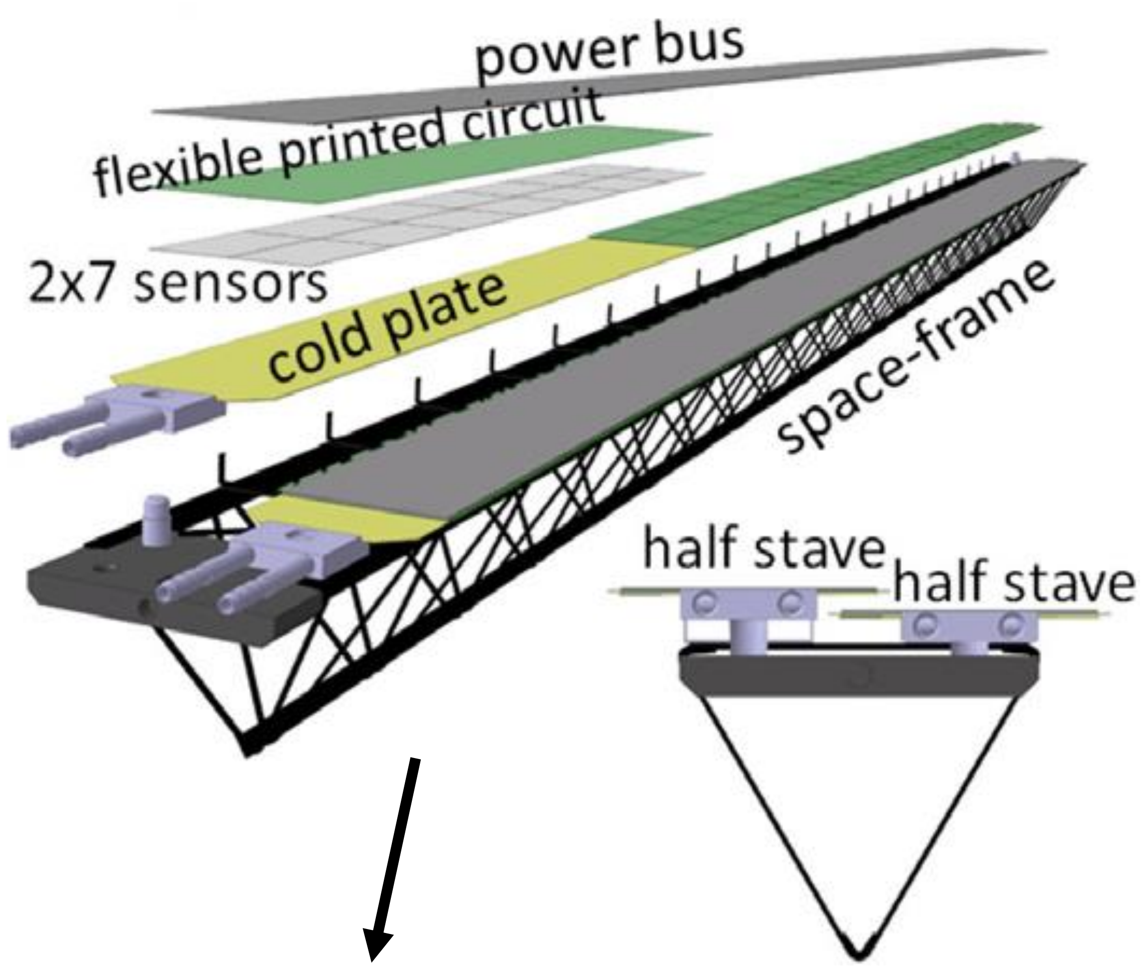




Yu. A. Murin and C. Ceballos, ***"The Inner Tracking System for the MPD Setup of the NICA Collider"***, Phys. Part. Nuclei 52, 742–751 (2021).

Components for building ITS by - OB:2028 & OB+IB:2029/30

The MAPS chip - MICA

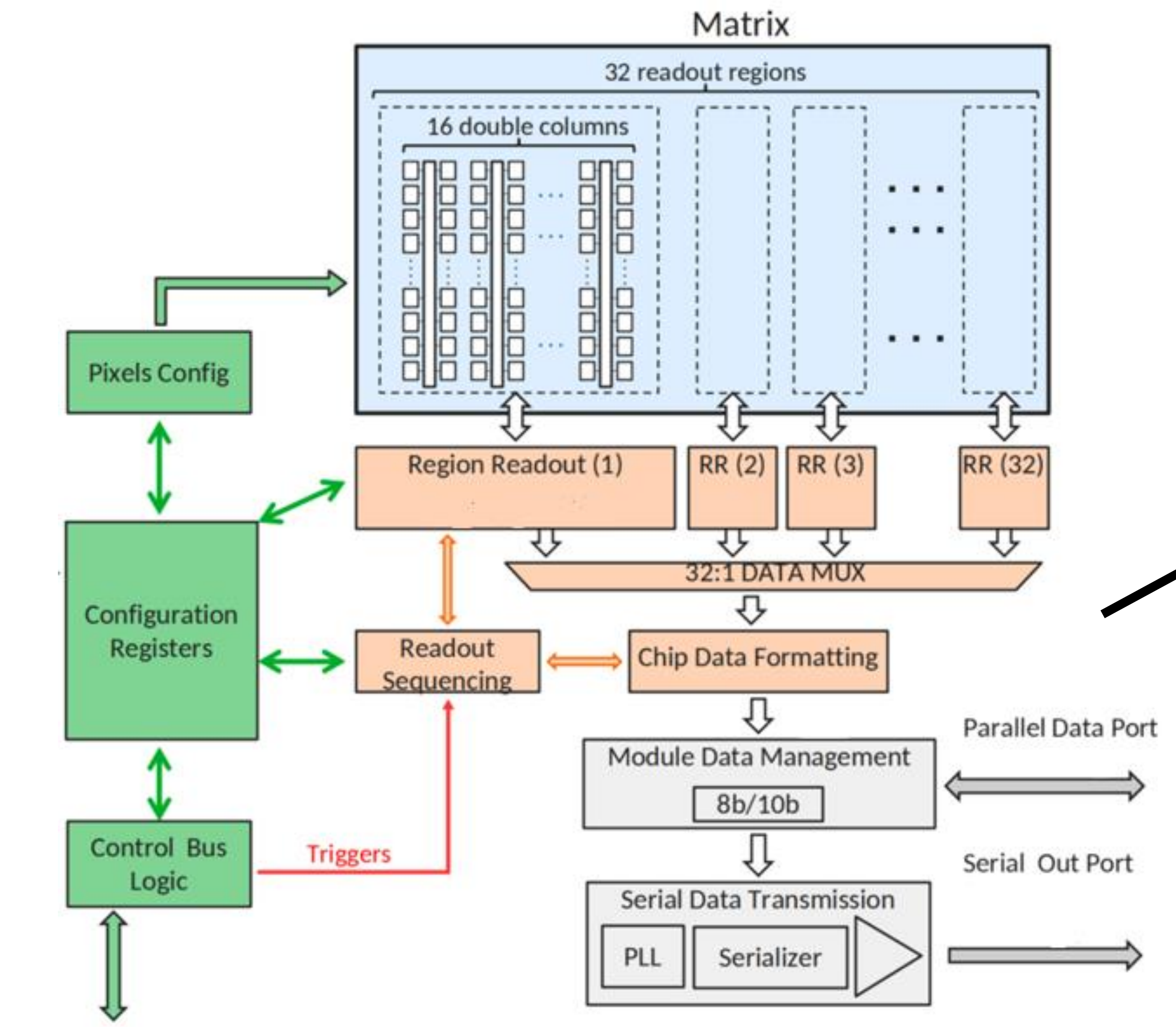


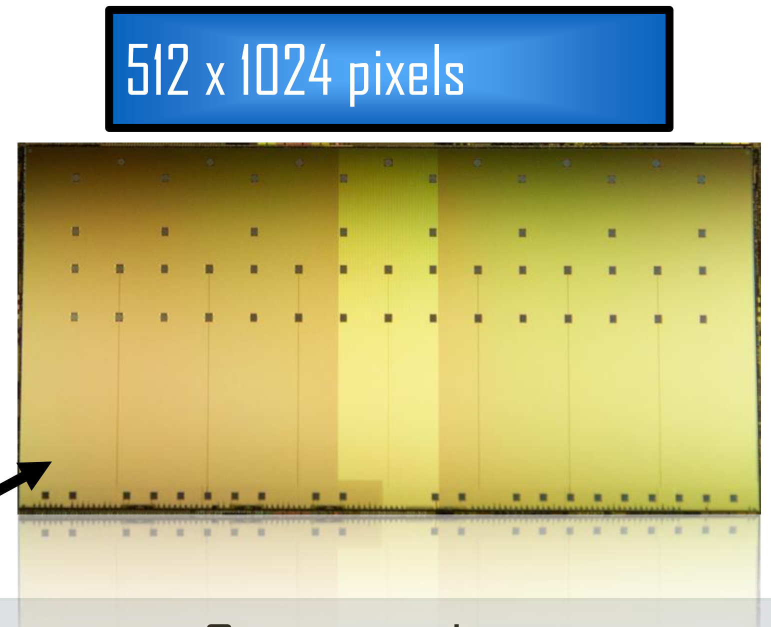
PRC FAB 0.13 μm CMOS pixel sensor first prototype

» High-resistivity (> 1kΩ cm) p-type substrate (500μm thick later to be thinned)

» Small n-well diode (2-3 μm diameter), ~100 times smaller than pixel => low capacitance.

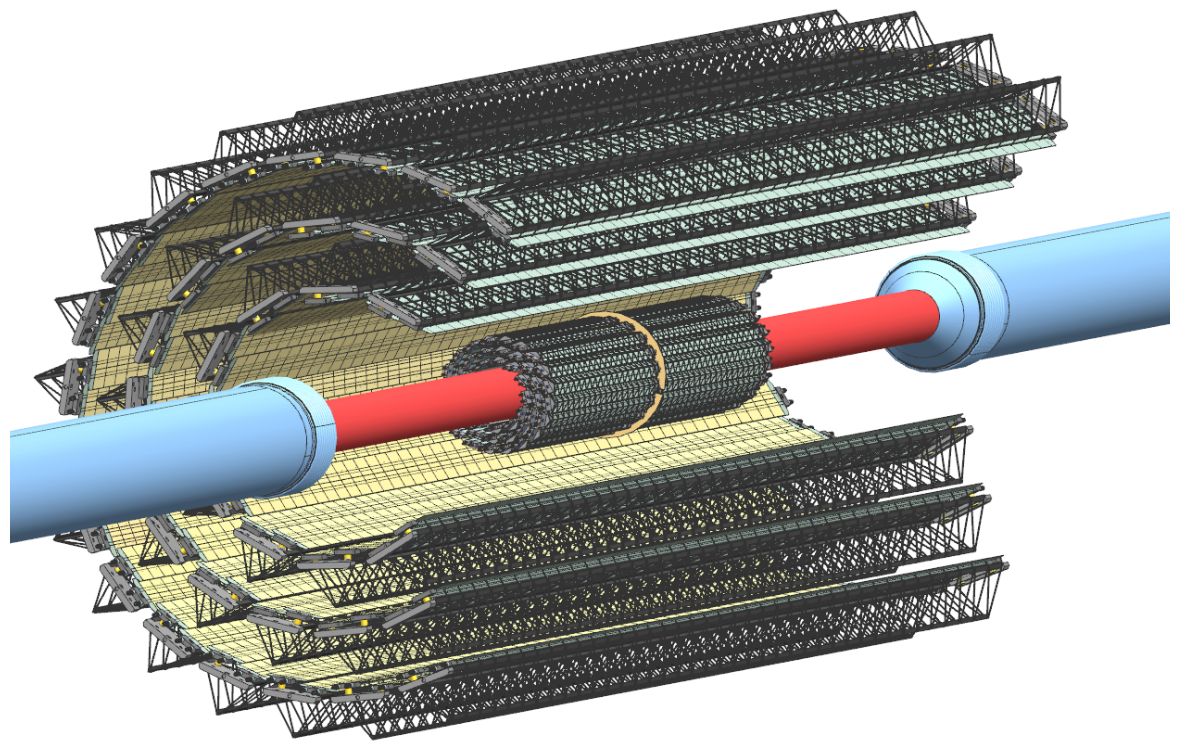
» Deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area.

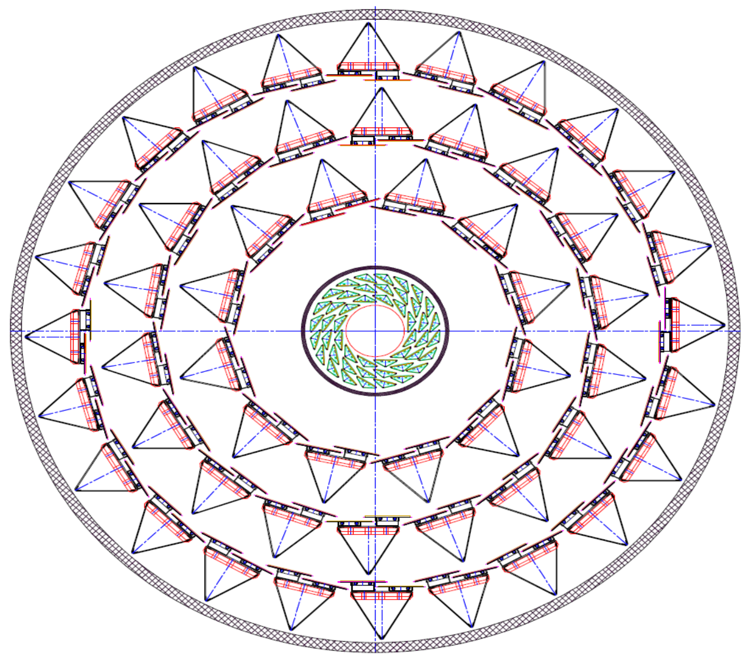




Sensor architecture

Size: 15mm x 30mm
Pixel pitch: 30.53μm x 26.8μm
Peaking time: < 1μs
Integral time: 5-10 μs
Power consumption: 30.5nA/pixel
Dead area 1.1mm x 30mm





OB = 54 Staves

Total number chips

10584 pcs

IB = 2x 48 Staves

Total number chips

864 pcs

Total number pixels

5,724 10^9

MPD ITS computer simulations - predictions for open charm identification

MPD - ITS

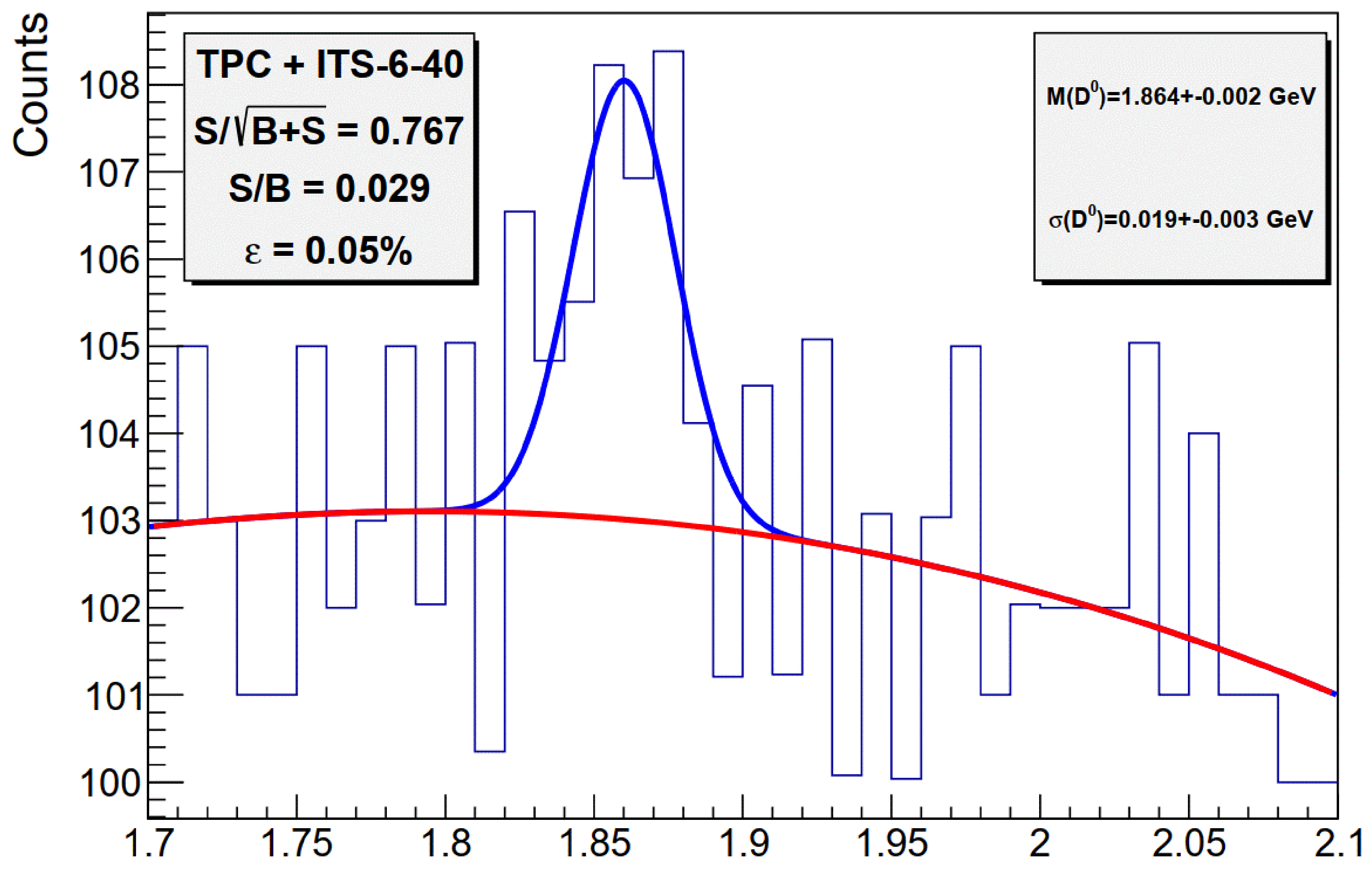
NICA

10,8 GeV Bi+Bi: D^+ and D^0 reconstruction using KF with TPC-TOF PID

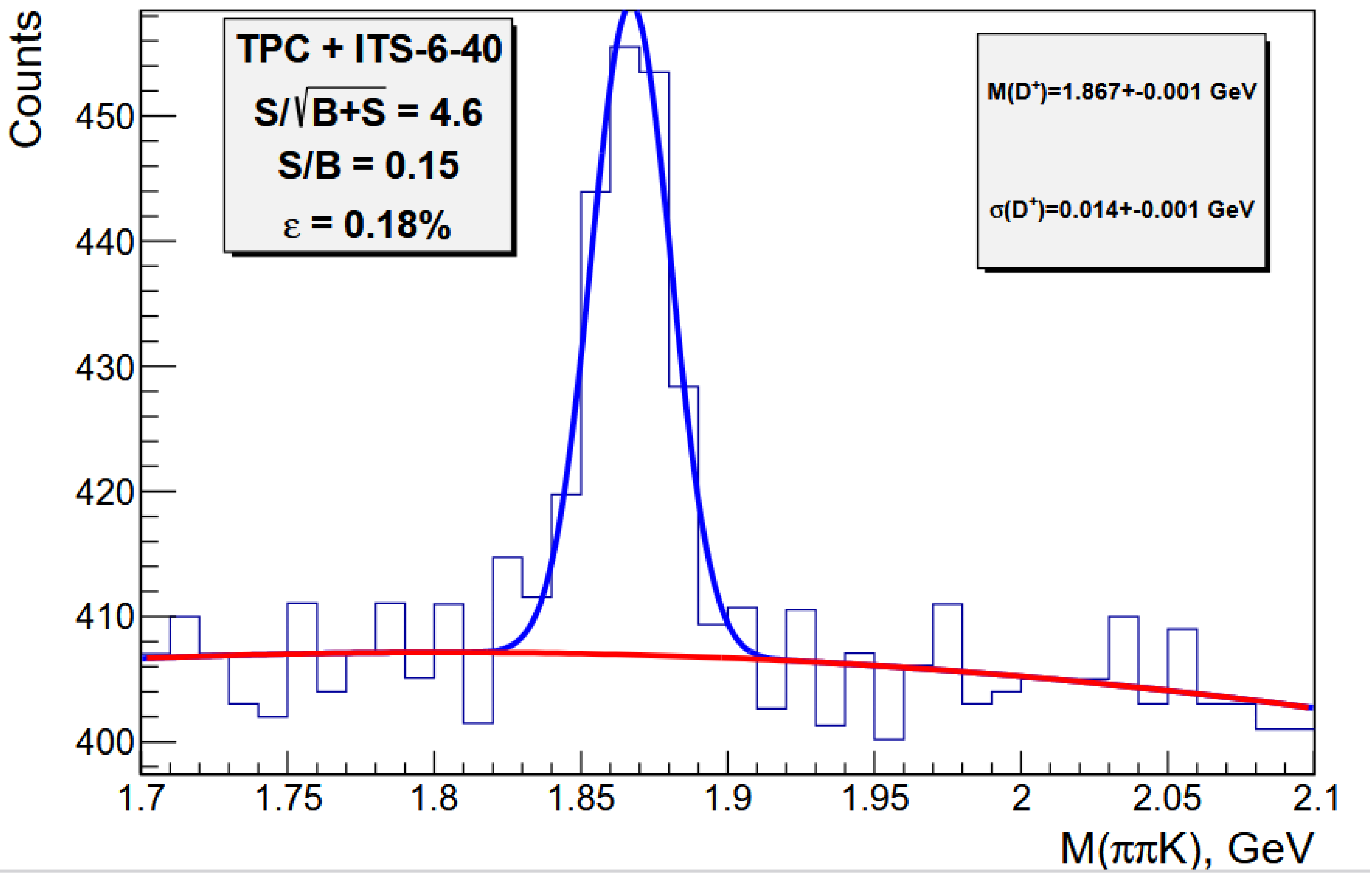
$D^0 \rightarrow K^- + \pi^+$

$D^+ \rightarrow K^- + \pi^+ + \pi^+$

M(πK): signal+background(100M)



M(ππK): signal+background(100M)



Particle	Decay Channel	cτ (μm)
D^0	$K^- \pi^+$ (3.8%)	123
D^+	$K^- \pi^+ \pi^+$ (9.5%)	312
D_s^+	$K^+ K^- \pi^+$ (5.2%)	150
Λ_c^+	$p K^- \pi^+$ (5.0%)	60

Preliminary results show that using the optimal BDT cut allows to reconstruct D^+ and D^0 with an efficiency of **0.18%** and **0.05%** respectively.

N_D = 3 444 mesons/month for $D^+ \rightarrow K^- + \pi^+ + \pi^+$

N_D = 406 mesons/month for $D^0 \rightarrow K^- + \pi^+$

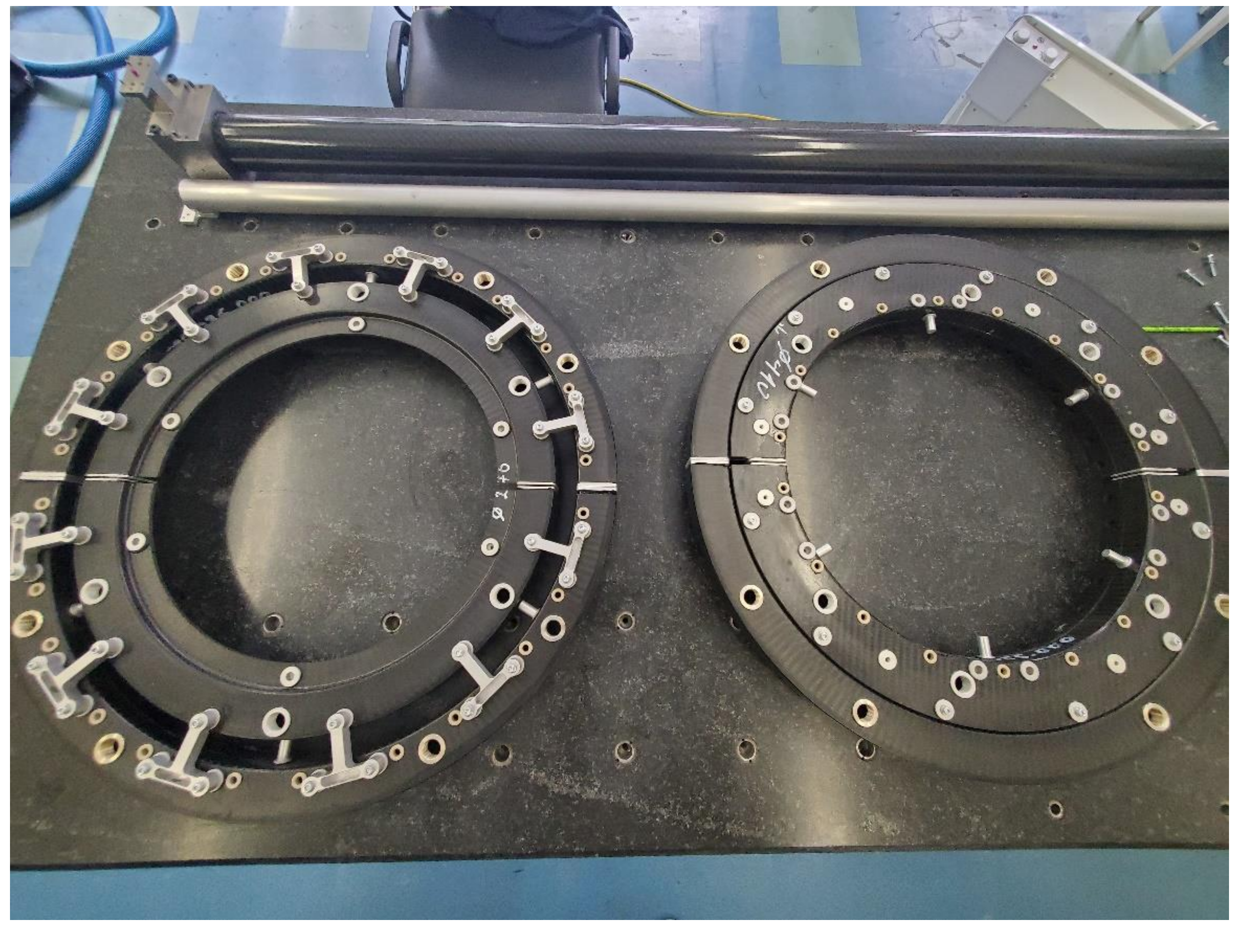
V.Kondratiev, E.Tsapulina, Y.Murin

Status of the ITS mechanics

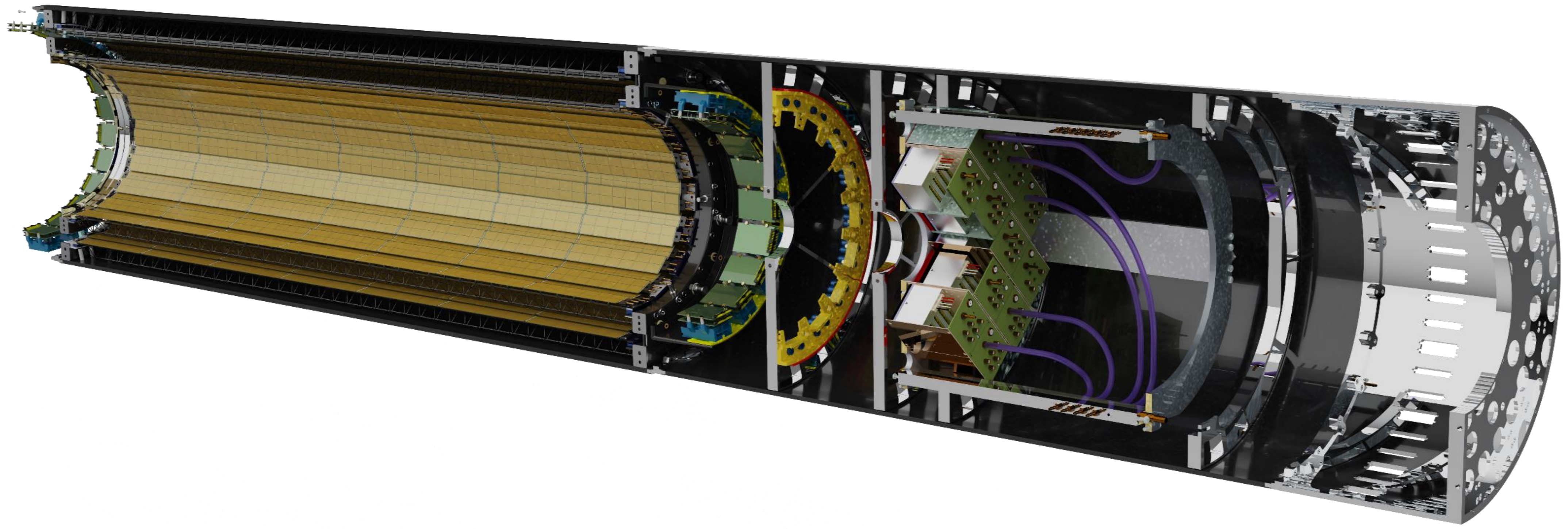
ITS mechanics works are focused on:

- mechanics of the ITS tracker,
- Installation Container

Thermal bridges for water cooling



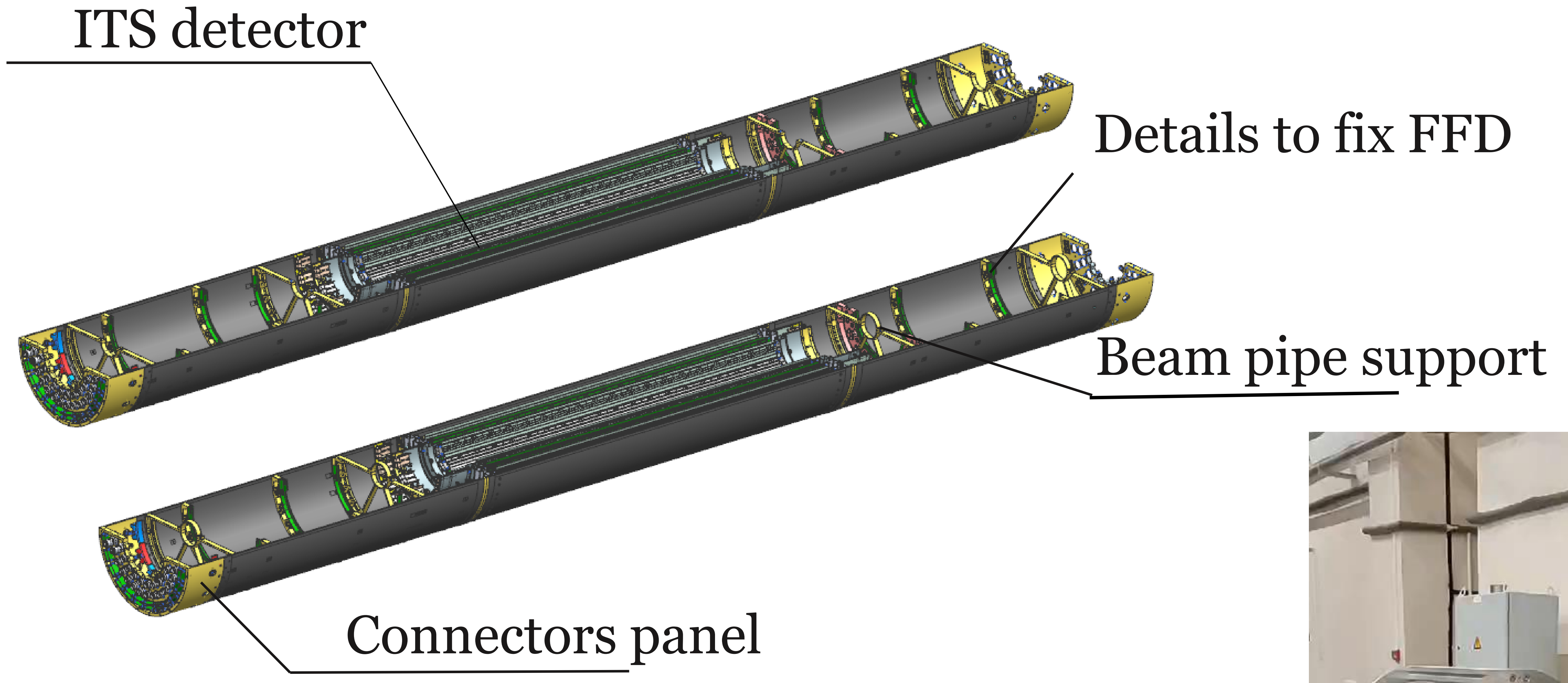
Support rings of the ITS

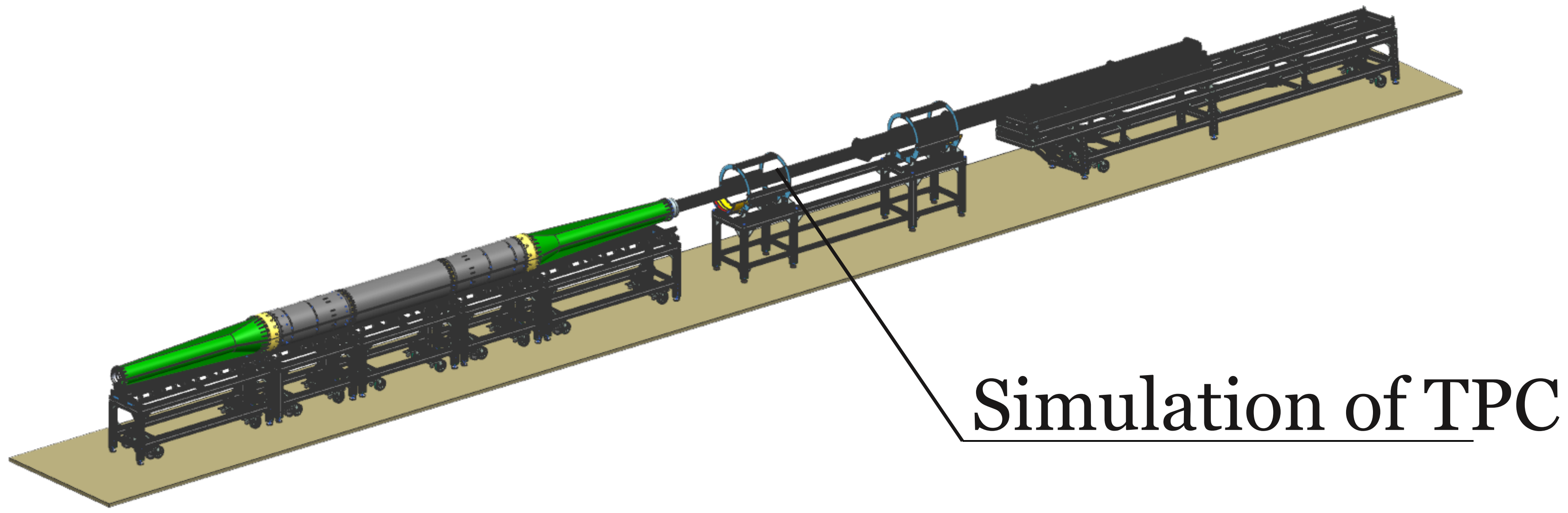


Installation container to place the FFD, ITS and the beam pipe and integrate it into the MPD

Status of the ITS mechanics

The assembly process of the Installation Container





Installation Container is 90% ready, readiness for integration into TPC is October 2025

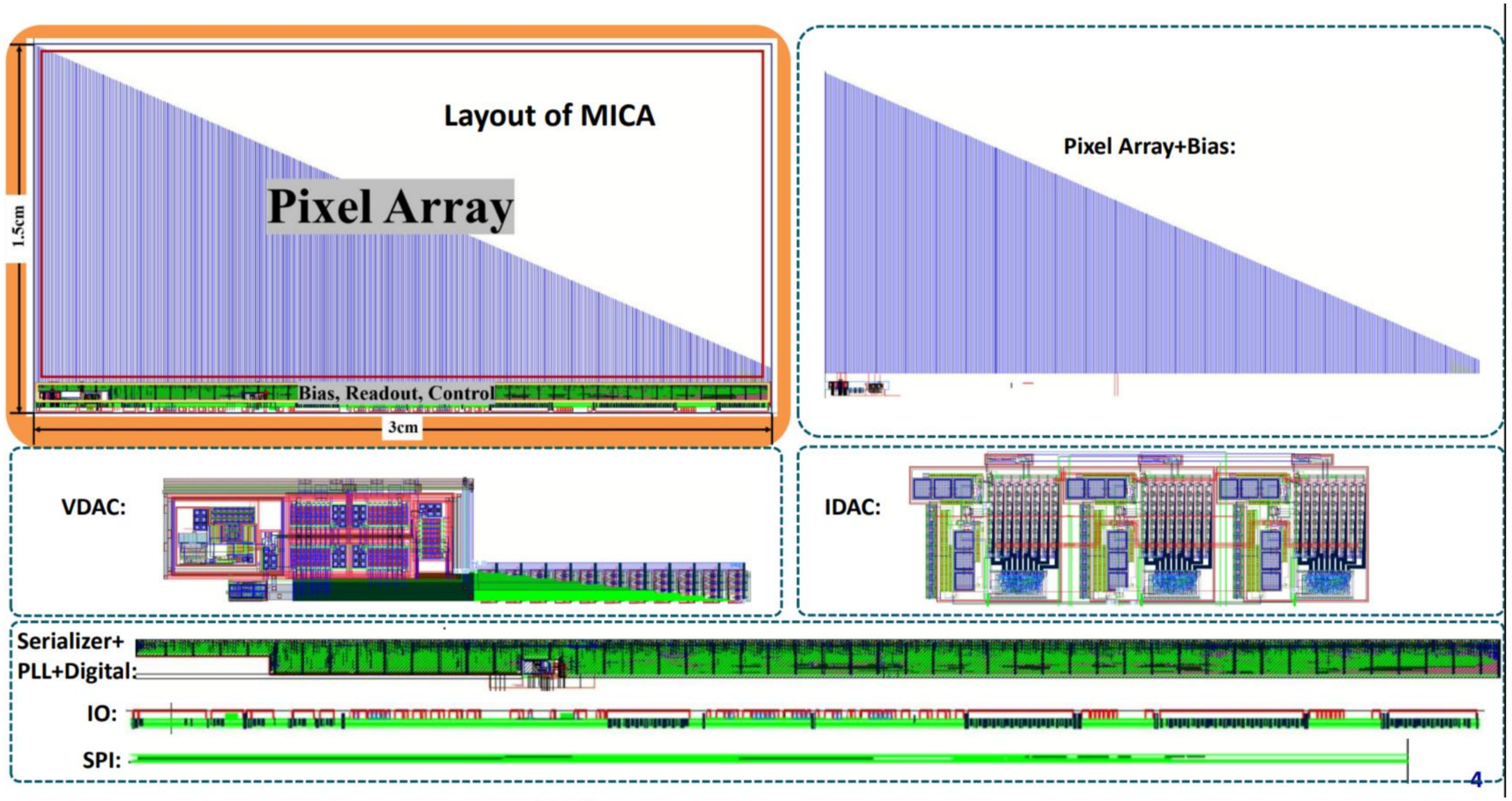
Working together for NICA MPD ITS

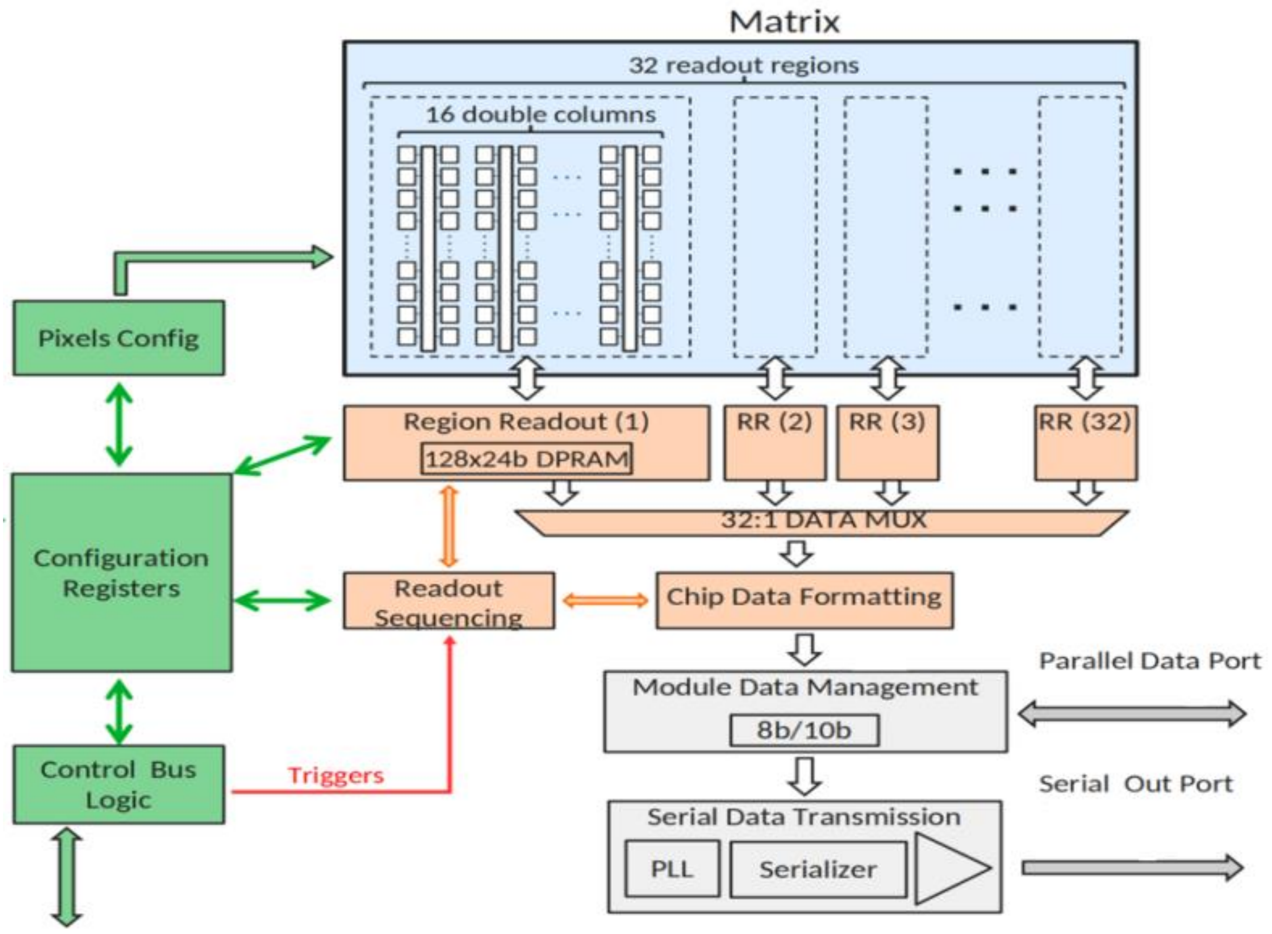
In order to further cooperate between JINR and Chinese institutions, the "NICA MPD-ITS Consortium" has been established:

- the acting time for the consortium is 5 years;
- the coordinator center within the Russian Federation will be the JINR and in China will be the CCNU
- the other institutions participating in the Consortium will have each one representative on the project structure for decision making and control.

Yu. A. Murin, C. Ceballos Sanchez for the MPD-ITS Collaboration, *"Modern Microelectronics for MPD-ITS. Monolithic Active Pixel Sensors and Readout System"*, accepted for publication in the 4th issue of Phys. Part. and Nucl. in 2024

Research on 130nm Bulk CMOS Process Pixel Chip — MICA prototype



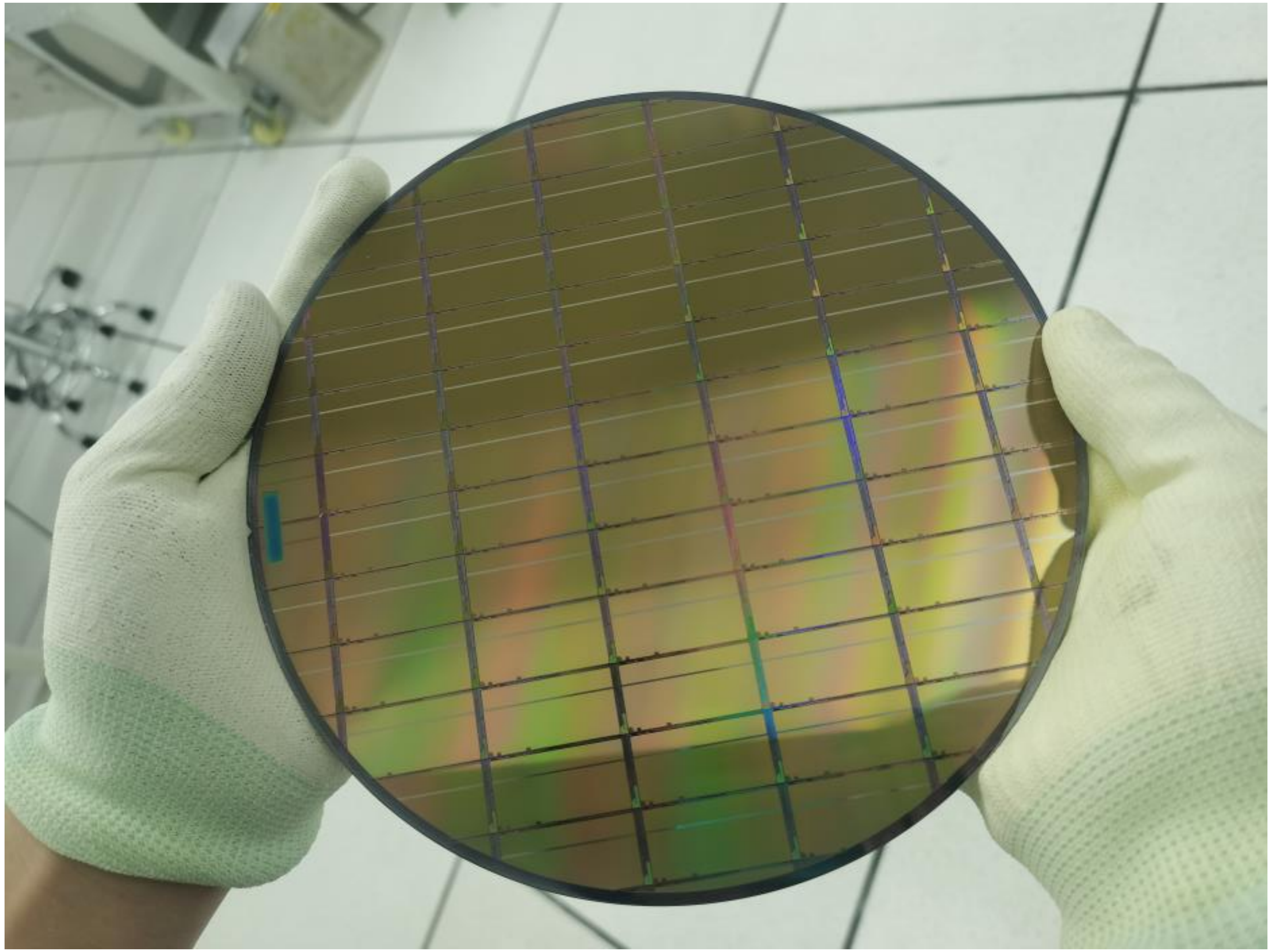


Fully functional MAPS chip MIC6_V3

- Process: 130 nm bulk CMOS
- Chip Size: 15mm x 30mm
- Pixel Array: 512 × 2x490
- Pixel Size: 30.53 μ m × 26.8 μ m
- Peaking Time: < 1us
- Integral Time: 5-10 us
- Parallel Data Port: 80 MHz I/O CMOS 3.3 V
- High Speed Serial Data Port: 1.1 Gb/s, 8B10B encoding
- Configuration Interface: SPI
- Two Readout Modes: trigger mode and continuous mode
- Single pixel can be masked; Pixel includes built-in testing functionality
- Zero Compression Readout

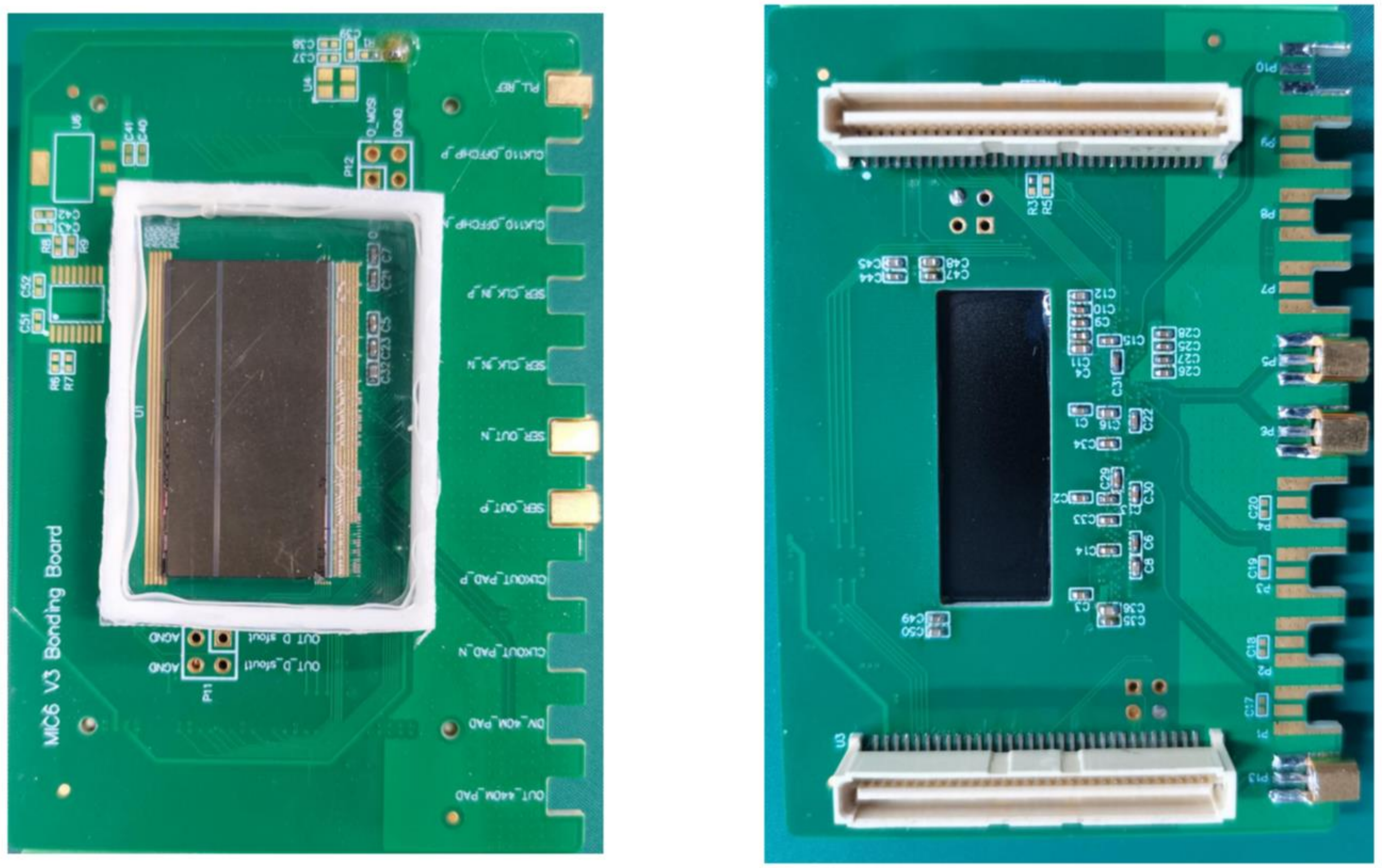
Courtesy of Prof. Xiangming Sun (CNNU), Wuhan

Research on 130nm Bulk CMOS Process Pixel Chip — MICA prototype

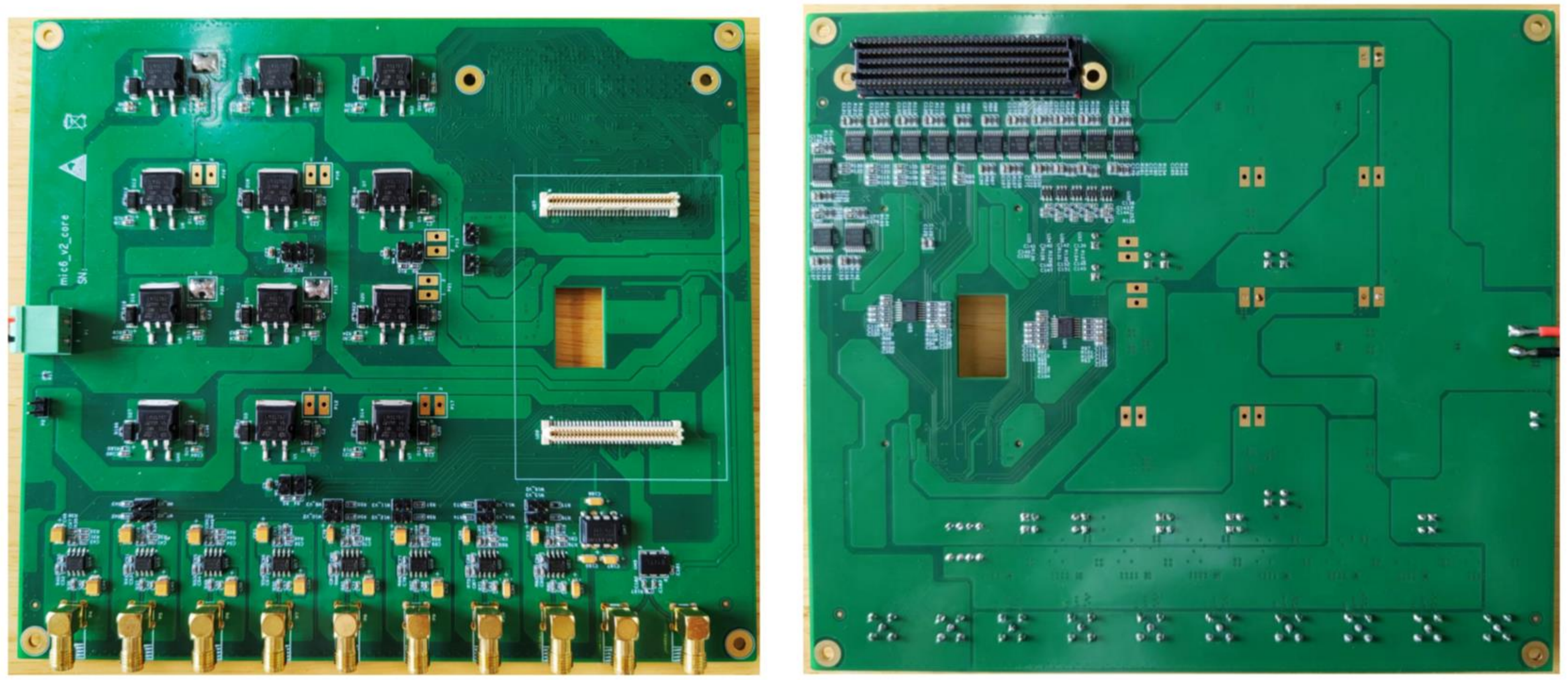


MICA prototype wafer photo

Courtesy of Prof. Xiangming Sun (CNNU), Wuhan

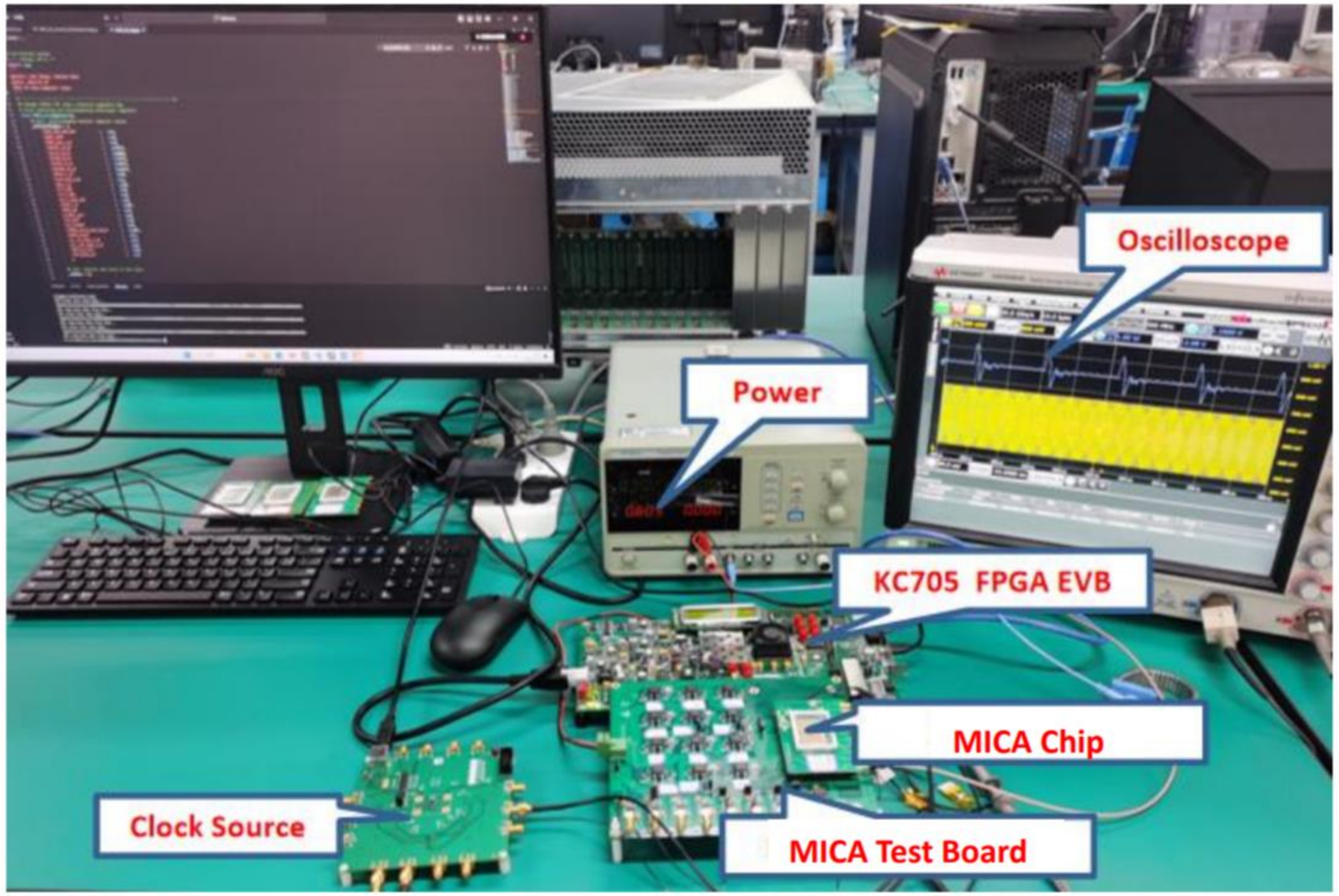


Photograph of the bonding board (front and back)



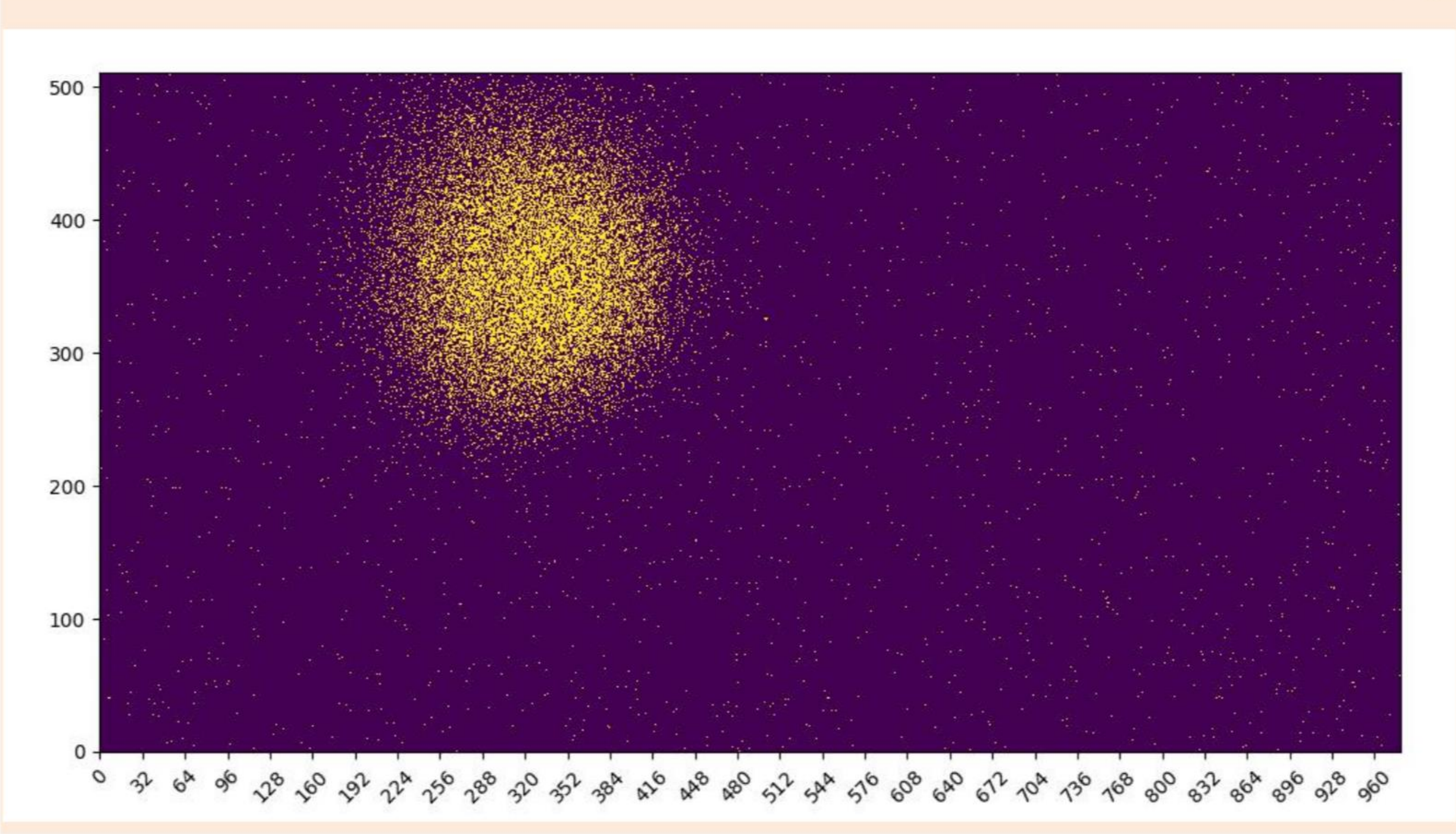
Photograph of the adapter board (front and back)

Research on 130nm Bulk CMOS Process Pixel Chip — MICA prototype



MICA chip test system

Test results-^{241}Am



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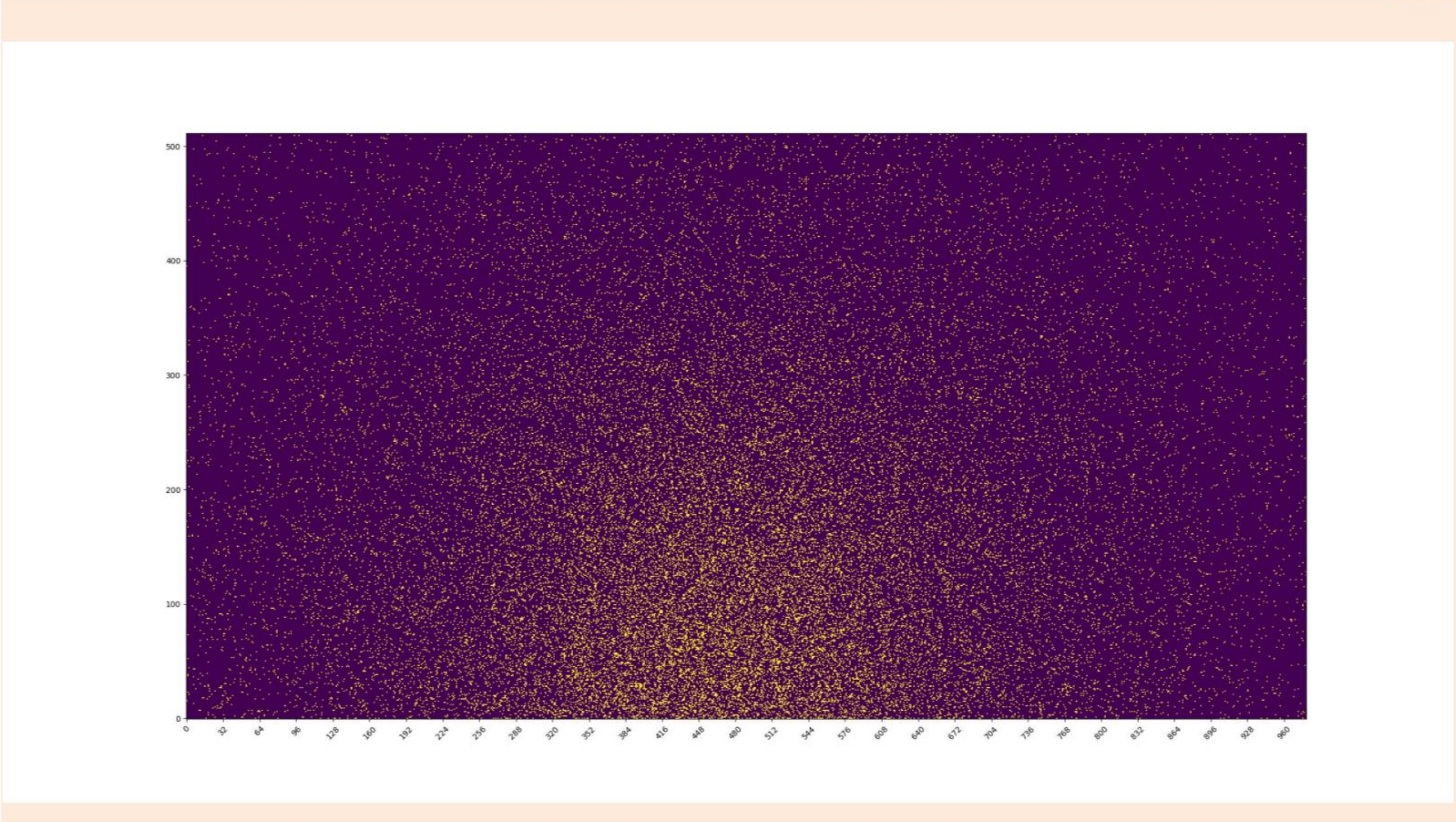
Test results-^{90}Sr



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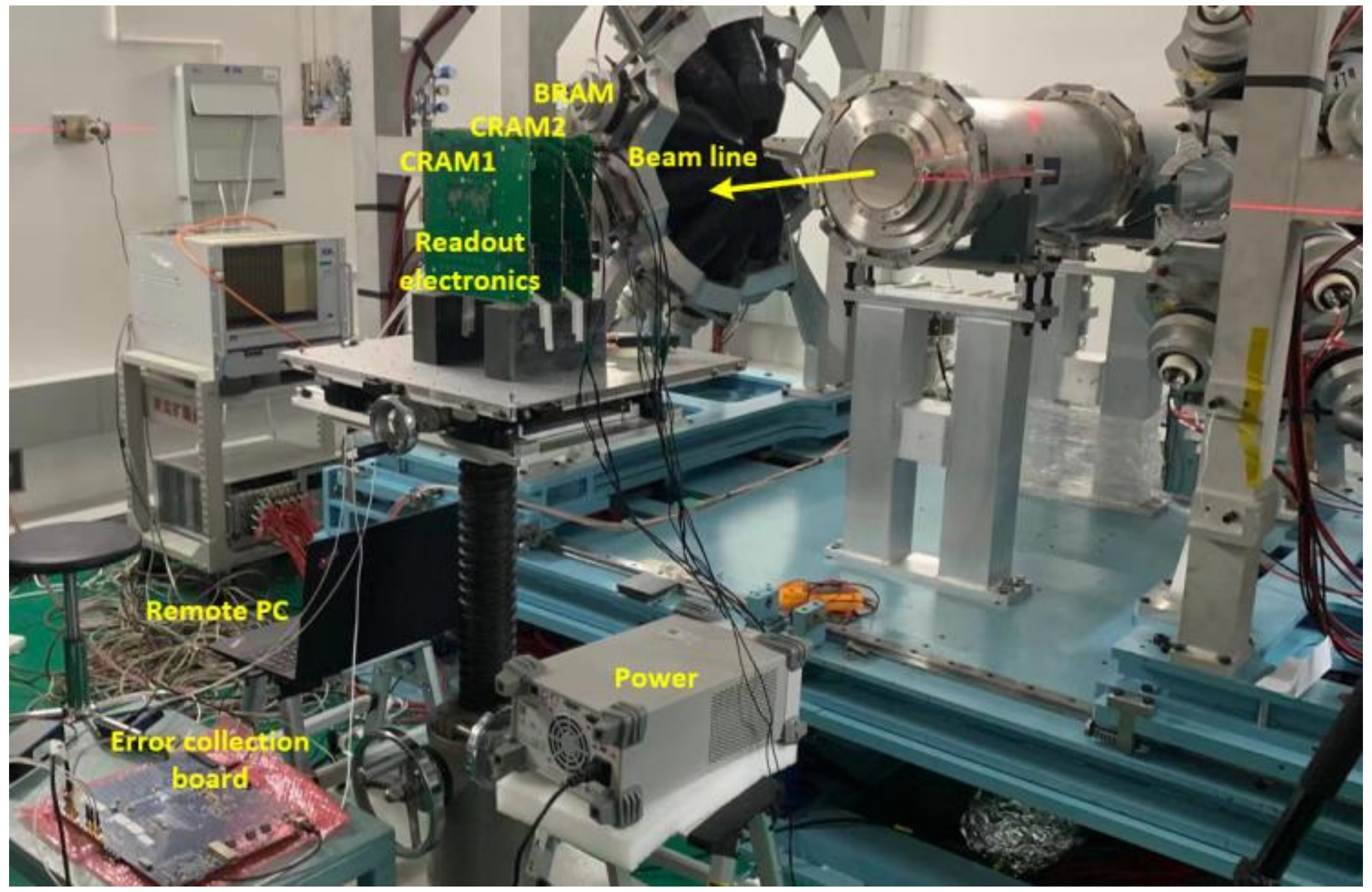
the MICA chip serial production will start in 2027 according to the current plan

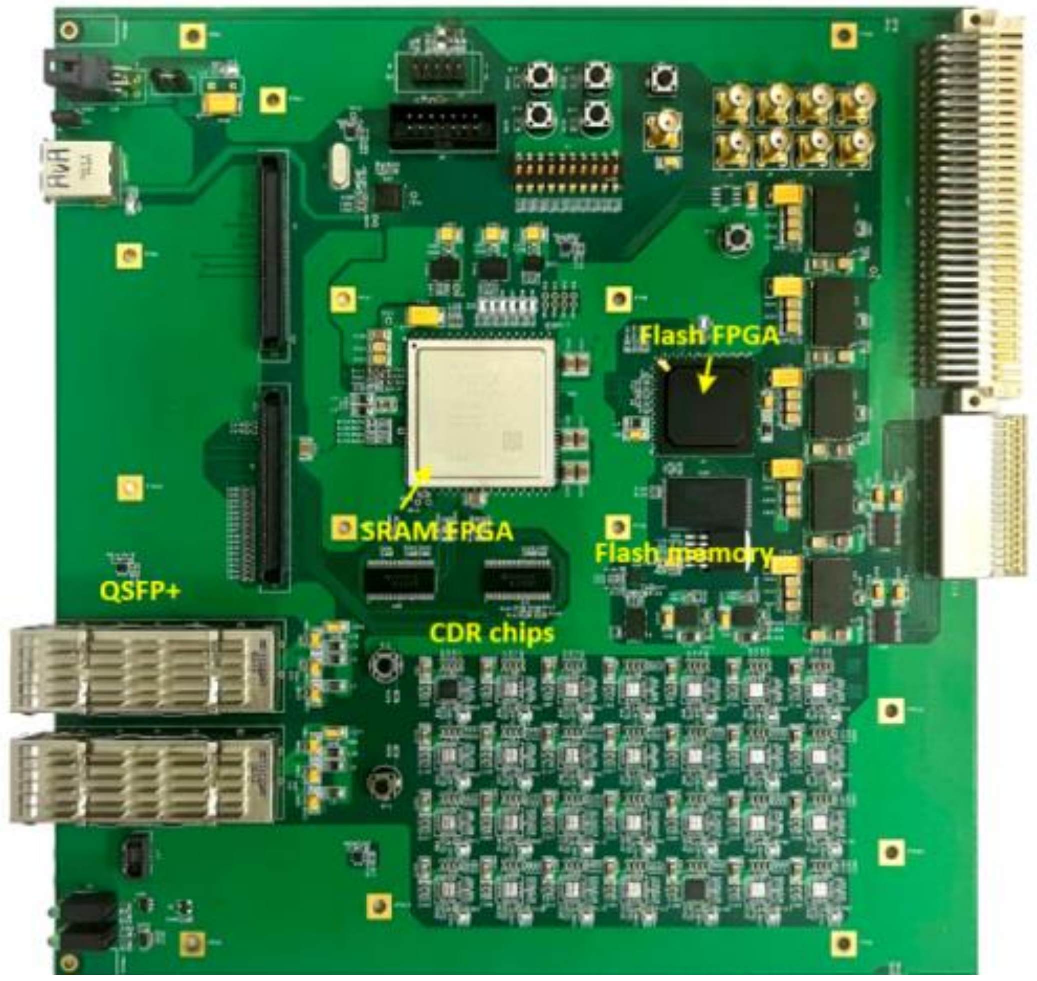
Courtesy of Prof. Xiangming Sun (CNNU), Wuhan

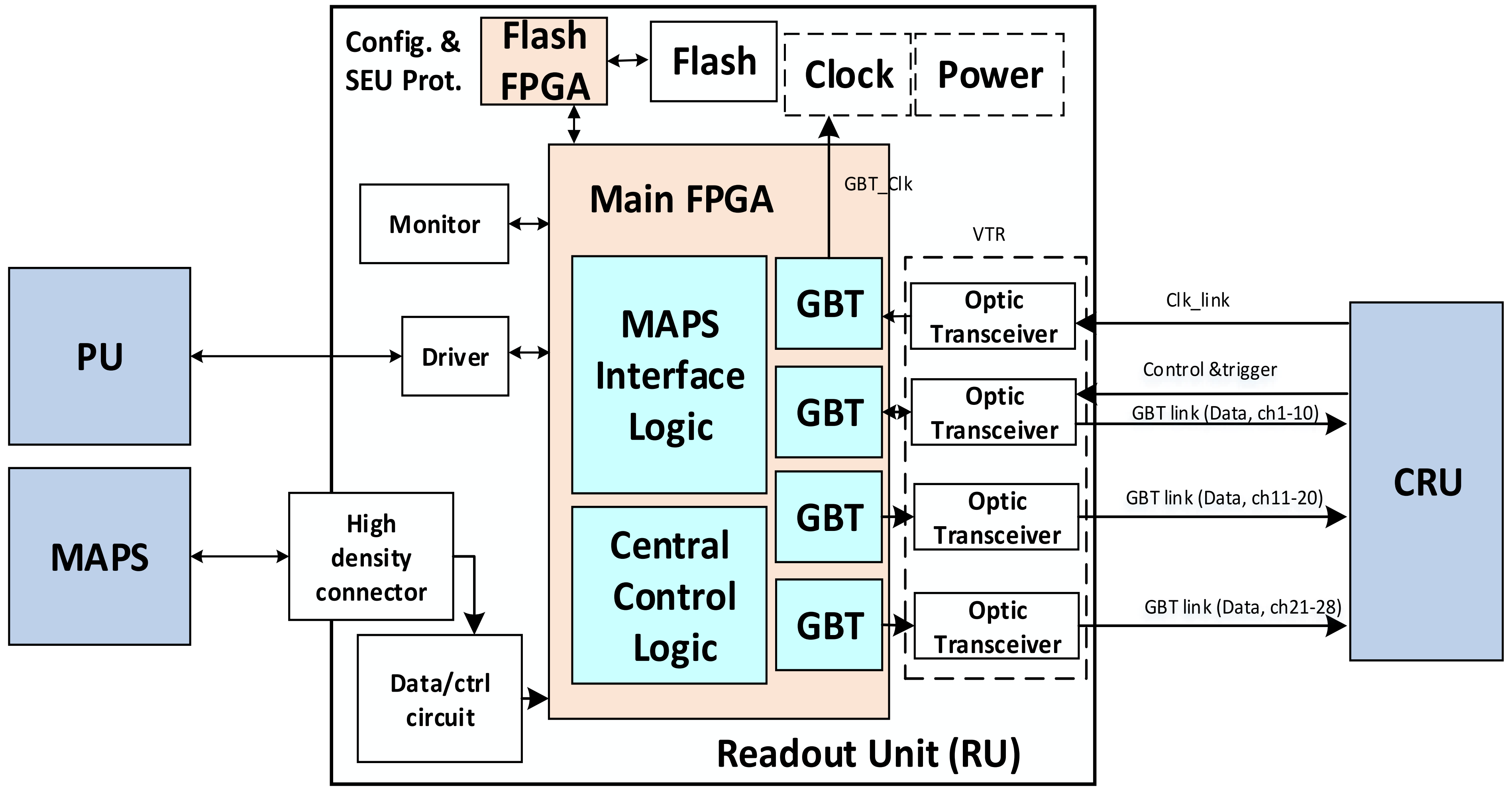
Readout Unit (RU) design by USTC

- The design of FPGA-based Readout Unit (RU) v.1 has been finished:
  - Transfer data and control signals from/to staves
  - FPGA implemented GBT protocol
  - Protection from SEU based on logic scrubbing, with a flash based FPGA
  - Power supply from VME backplane
- Laboratory test and beam test for v.1 was completed:
  - Input 400 MHz, ouput 5 Gbps, BER (bit error rate) $< 10^{-12}$
  - SEU events can always be detected and self-recovered.

NICA_ROC FPGA is planned to be finalized in a month (firmware modifications, adapted board implementation)



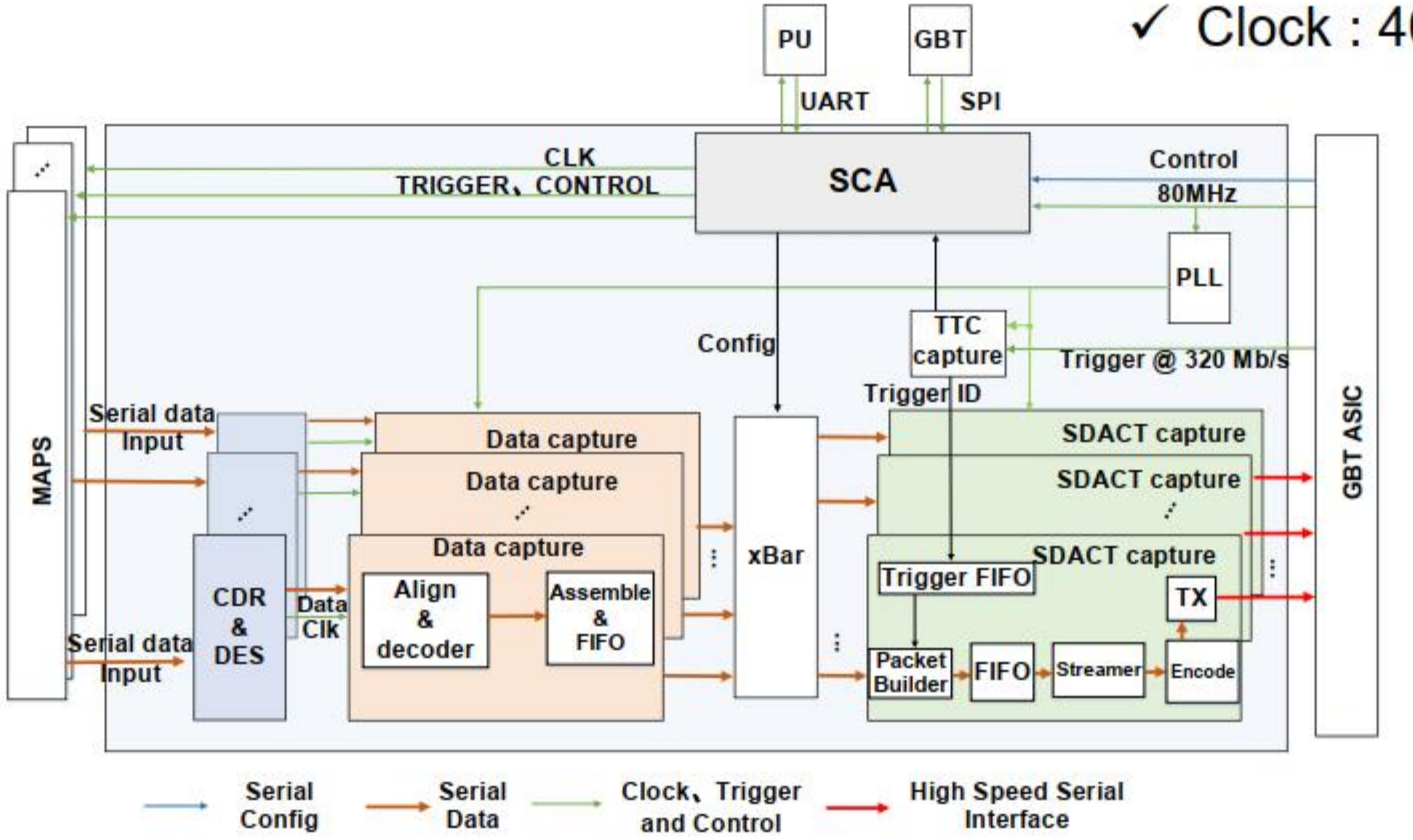




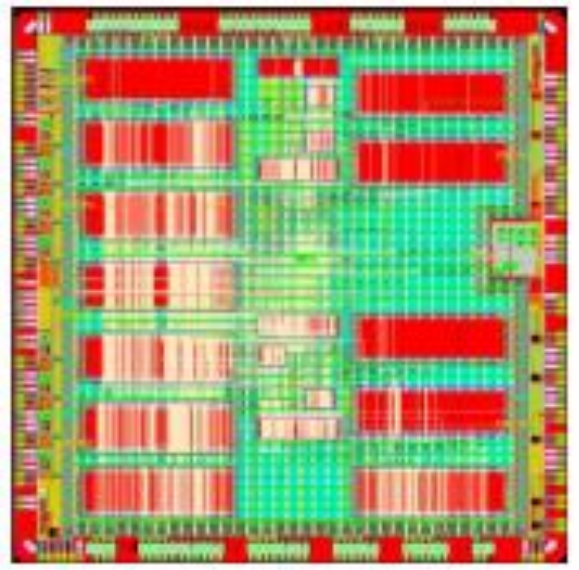
Courtesy of Prof. Lei Zhao (USTC), Hefei

NICA_ROC V1 ASIC by USTC

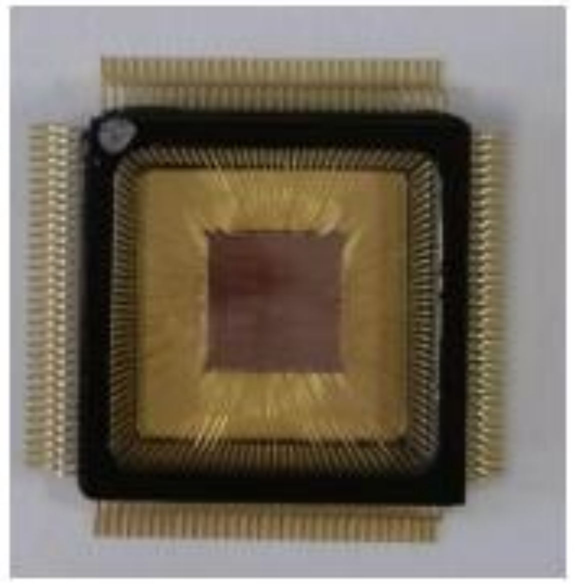
- MAPS Link:
  - ✓ Data link: 400 Mbps / 8 channels
  - ✓ Cfg link: 40 Mbps / Bi-directional
  - ✓ Clock : 40 MHz
- GBT Link:
  - ✓ Data link: 160/320 Mbps
    1/2/4 channels
  - ✓ Cfg link: 80 Mbps
  - ✓ Trigger link :320 Mbps
  - ✓ Clock : 40 MHz



UNIVERSITY OF SCIENCE AND TECHNOLOGY OF CHINA



5 mm×5 mm

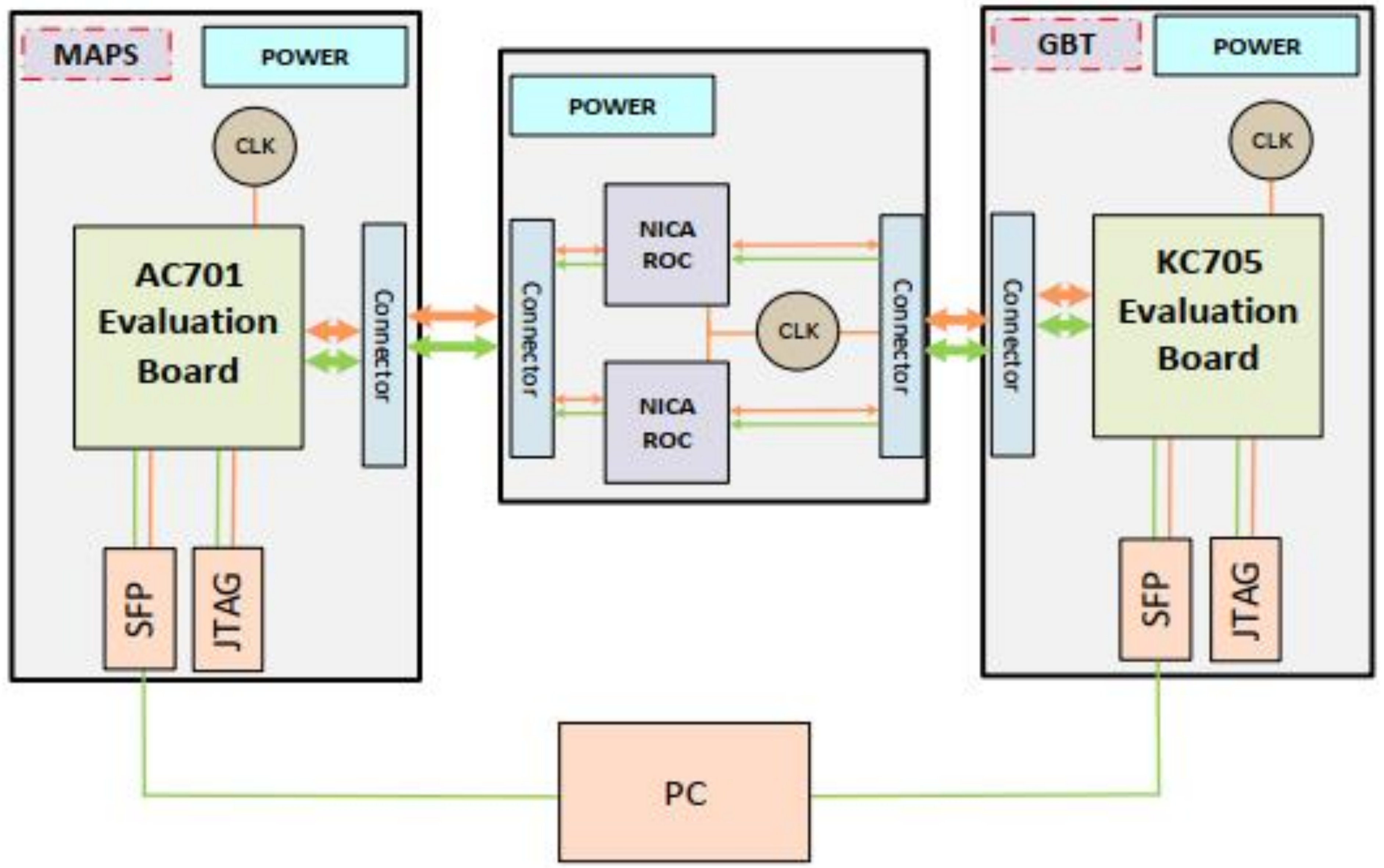


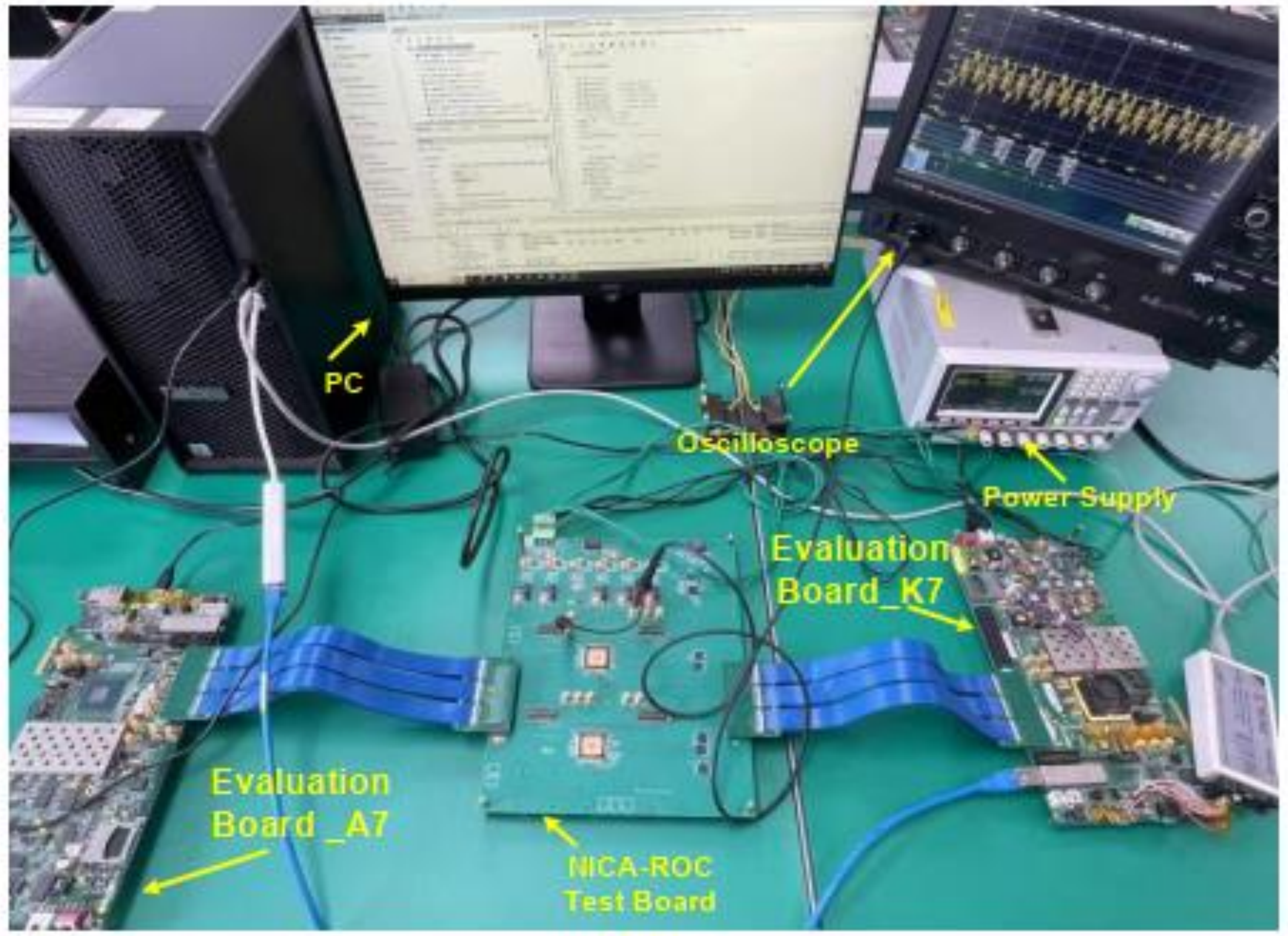
CQFP128

Courtesy of Prof. Lei Zhao (USTC), Hefei

NICA_ROC V1 ASIC by USTC – TEST SETUP

- Simulate the MAPS data using an evaluation board (AC701)
- Simulate the function of GBT chip using an evaluation board (KC705)





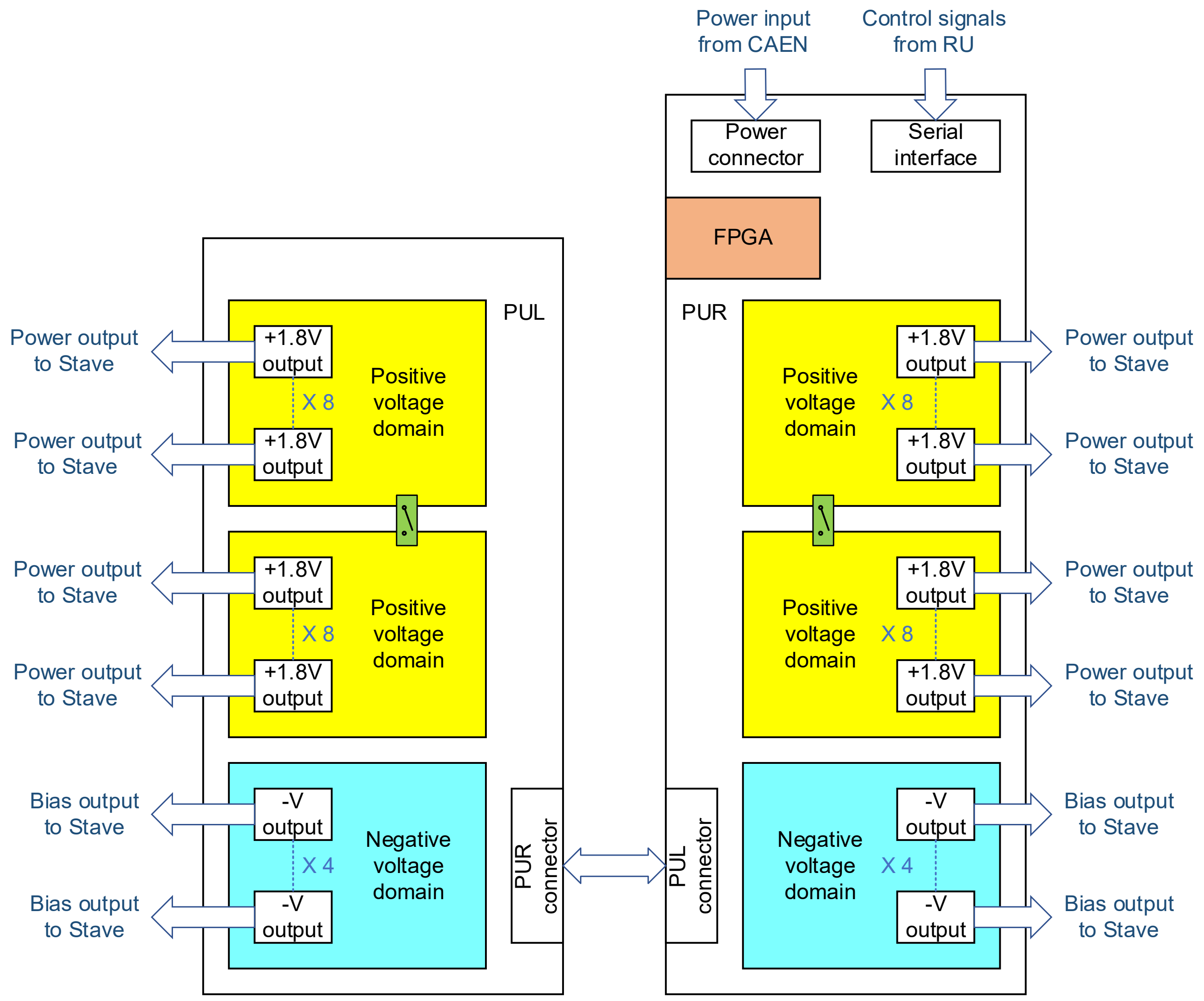
UNIVERSITY OF SCIENCE AND TECHNOLOGY OF CHINA

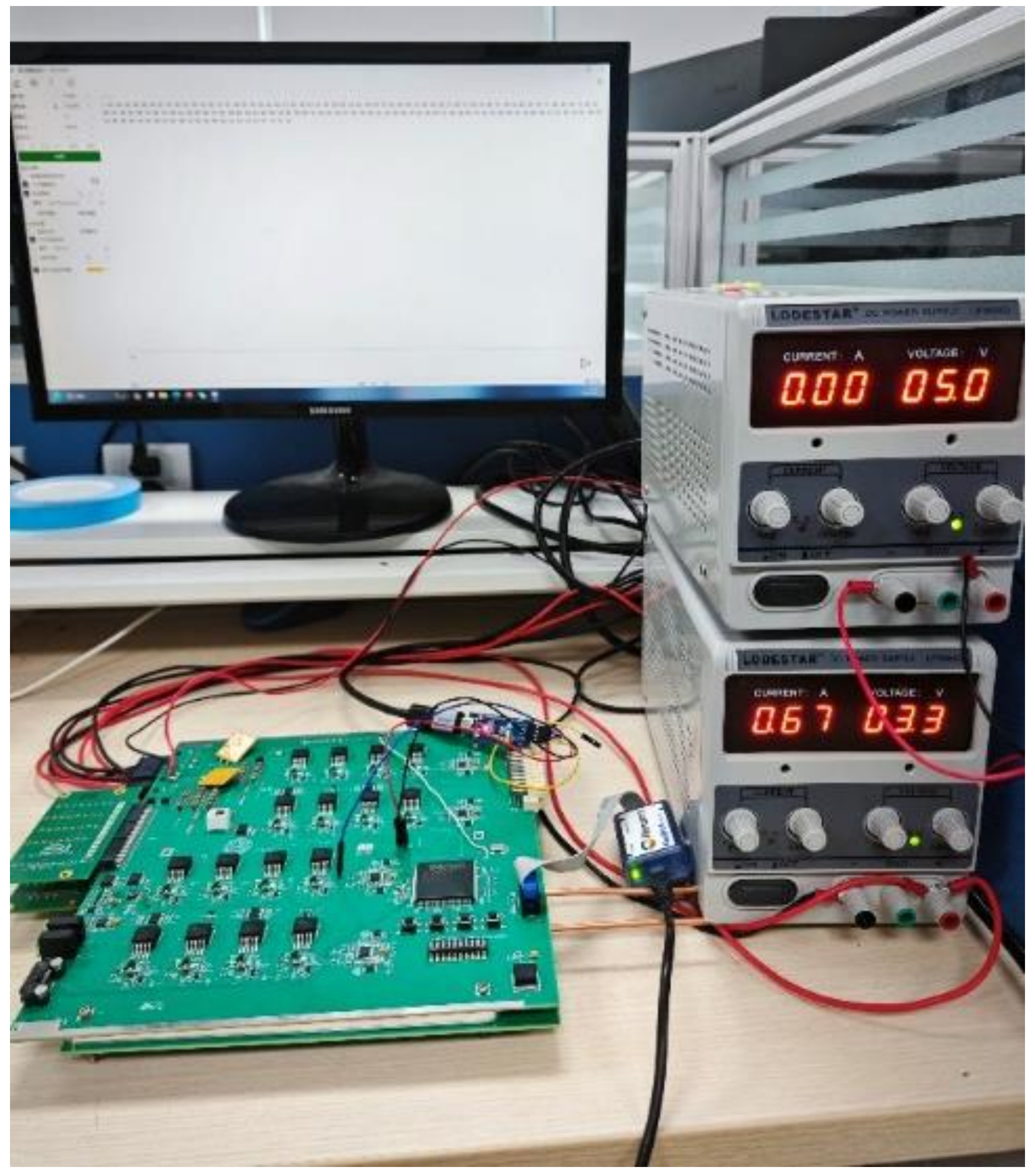
Courtesy of Prof. Lei Zhao (USTC), Hefei

Power Unit (PU) design by USTC

- The design of Power Unit (PU) has been finished
  - A power board (PB) consists of two independent PUs (PUR and PUL)
  - Each PU contains 8 channels of analog output (1.8V/250mA) and 8 channels of digital output (1.8V/1.5A)
  - A flash FPGA on PUR controls both PUR and PUL and is responsible for communication with RU
  - Real-time compensation for the voltage drop in power cable
- All desired functions have been tested in the laboratory successfully

PB is Ready for mass production



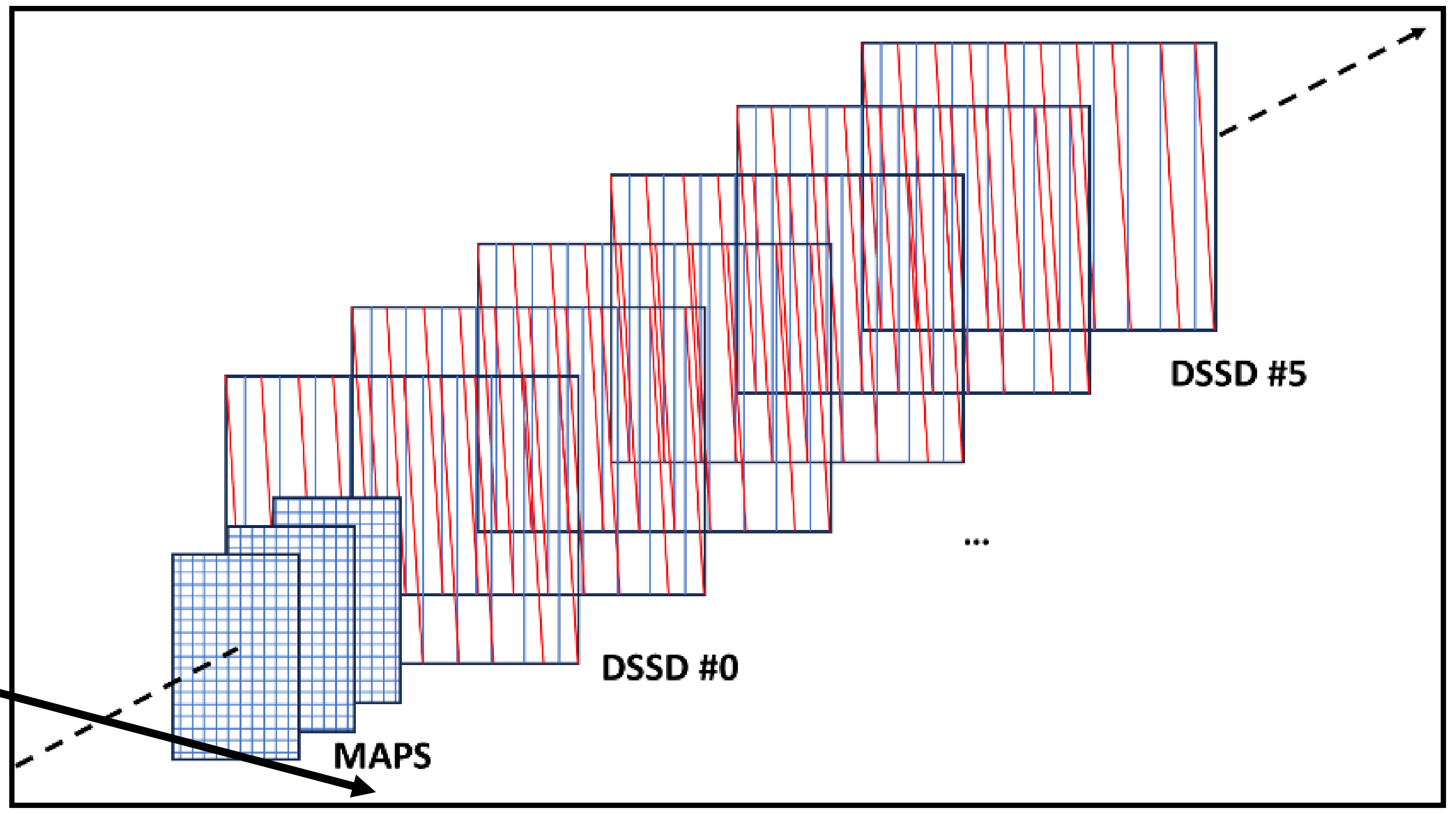


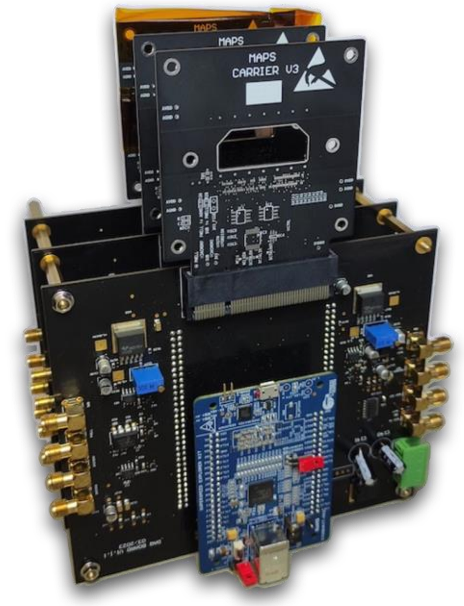
Courtesy of Prof. Lei Zhao (USTC) , Hefei

Preparations for the in-beam tests in Protvino and Gatchina

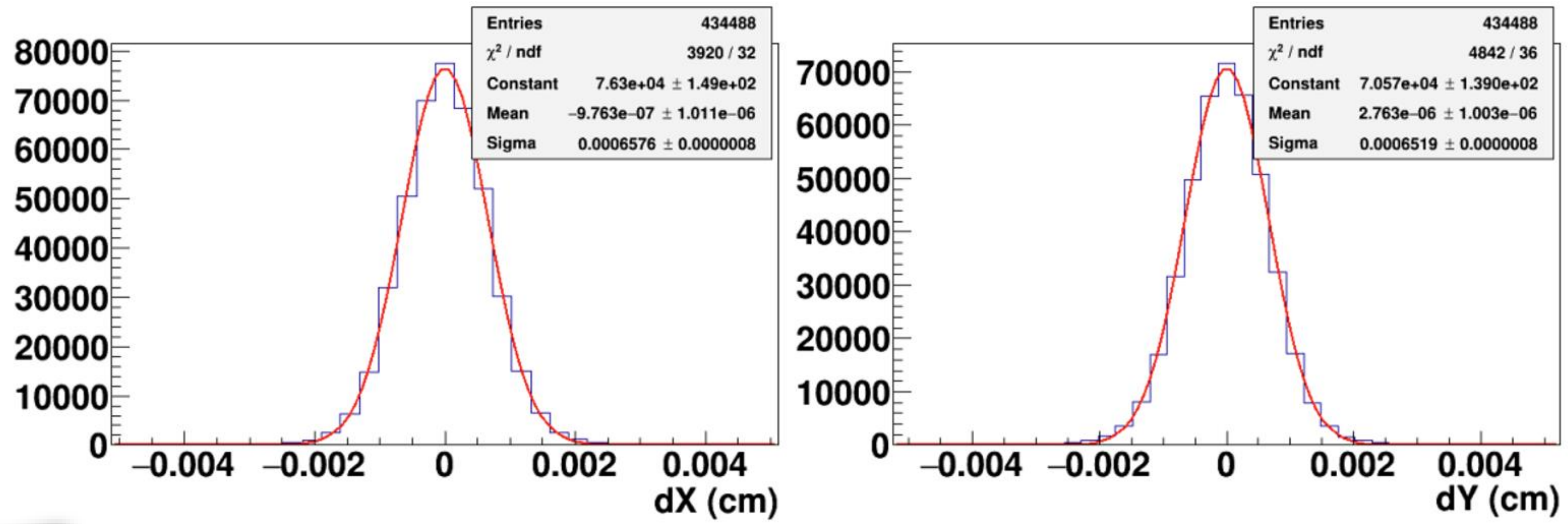
Tests with 1 GeV proton beam in Gatchina

DUT





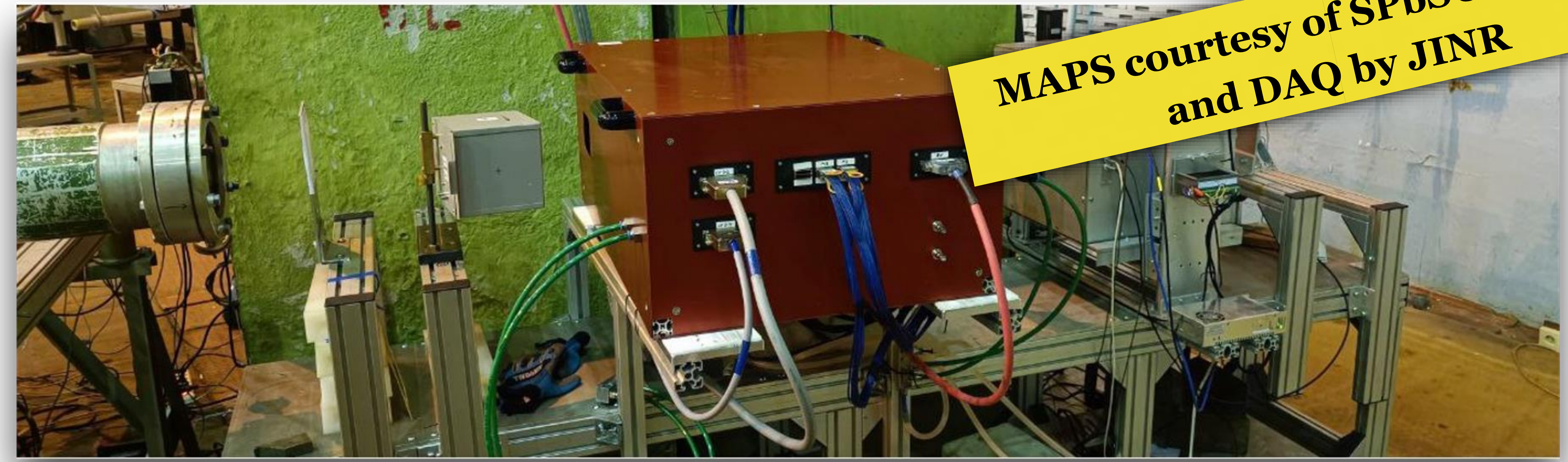
Residuals



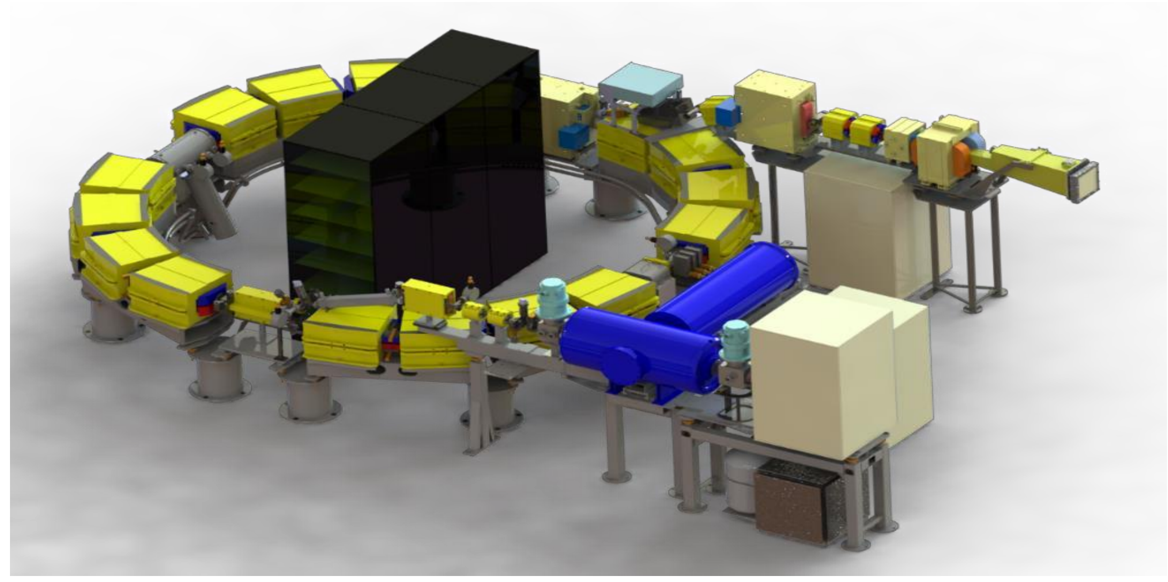
Residual X/Y = 6.58 um / 6.52 um;

Spatial resolution X/Y = 4.1±0.4 um /4.06 ± 0.4 um;,Efficiency > 99 %

MAPS courtesy of SPbSU readout and DAQ by JINR



Anticipated tests in Protvino with 150 – 300 MeV protons



PROTOM Ltd.

D.Dementiev,R.Arteche, M.Shitenkov,V.Leontiev, V.Kolazhvari

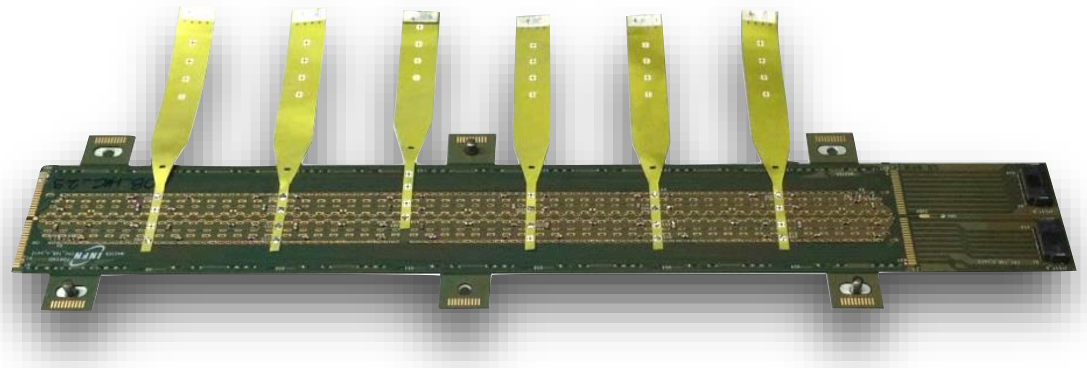
Module (HIC) and Supermodule(Staves) Assembly Readiness

Full technological transfer from ALICE to MPD

- Complete KnowHow
- Detector assembly and testing hardware/software
- Supervision and support from ALICE specialists

} Setup at JINR of the full detector assembly line from chips to detector layers

FPC



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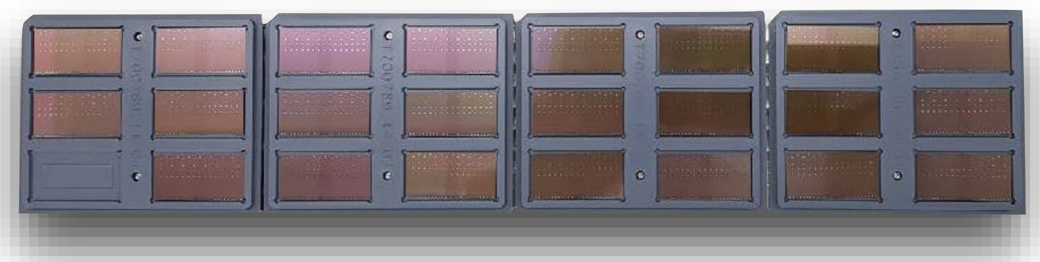
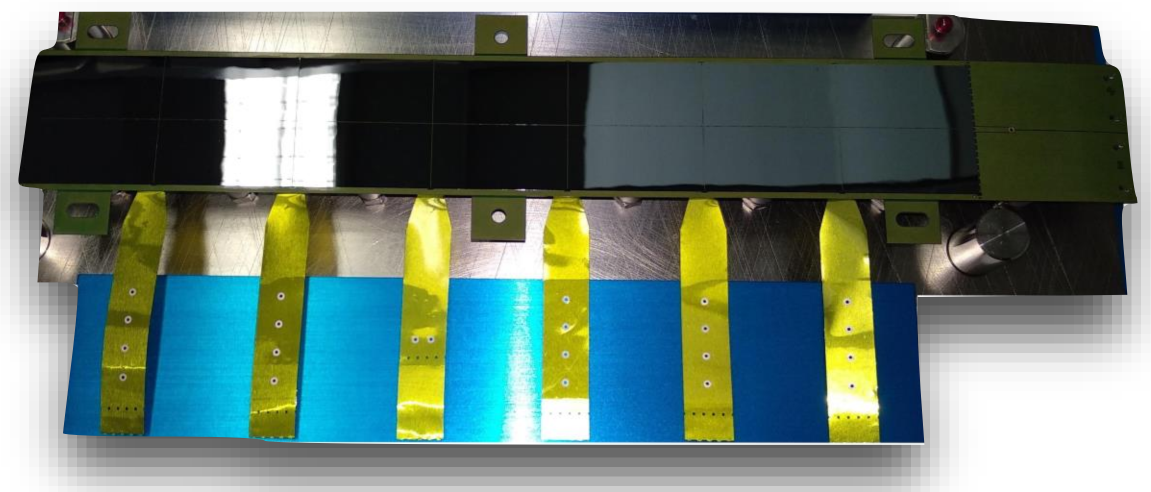
MAPS



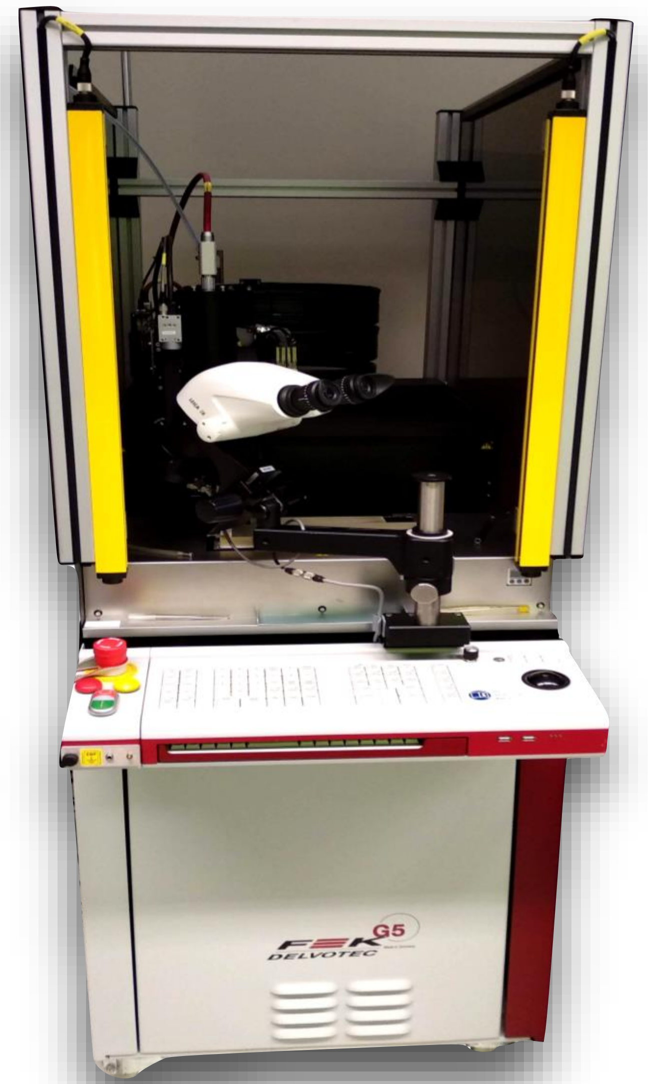
↓

HIC

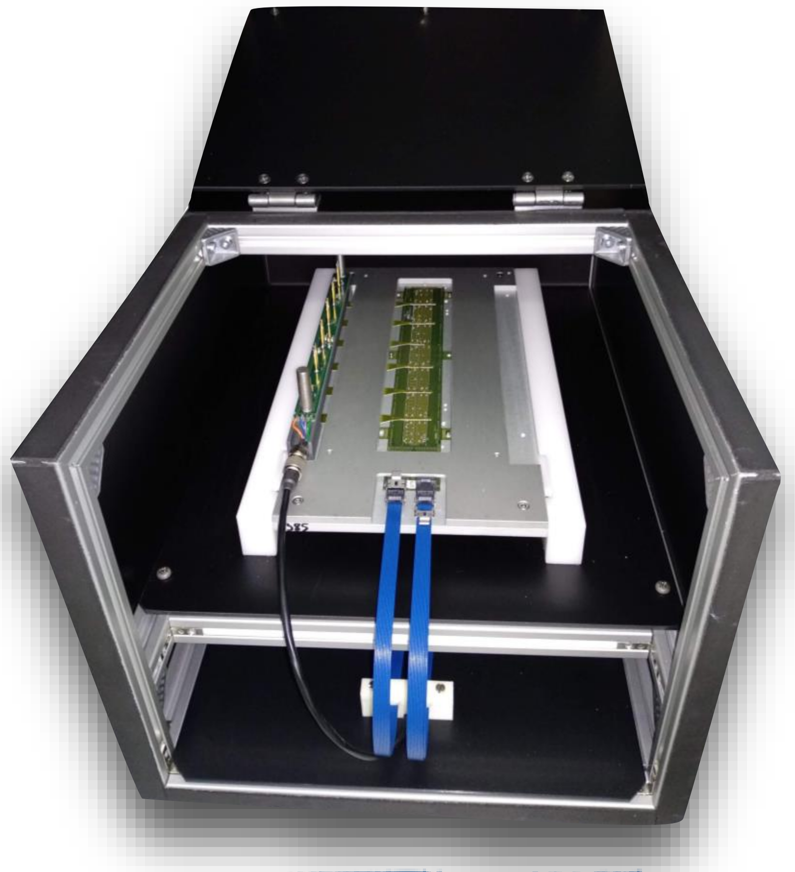


Chips selection

Chips alignment and gluing



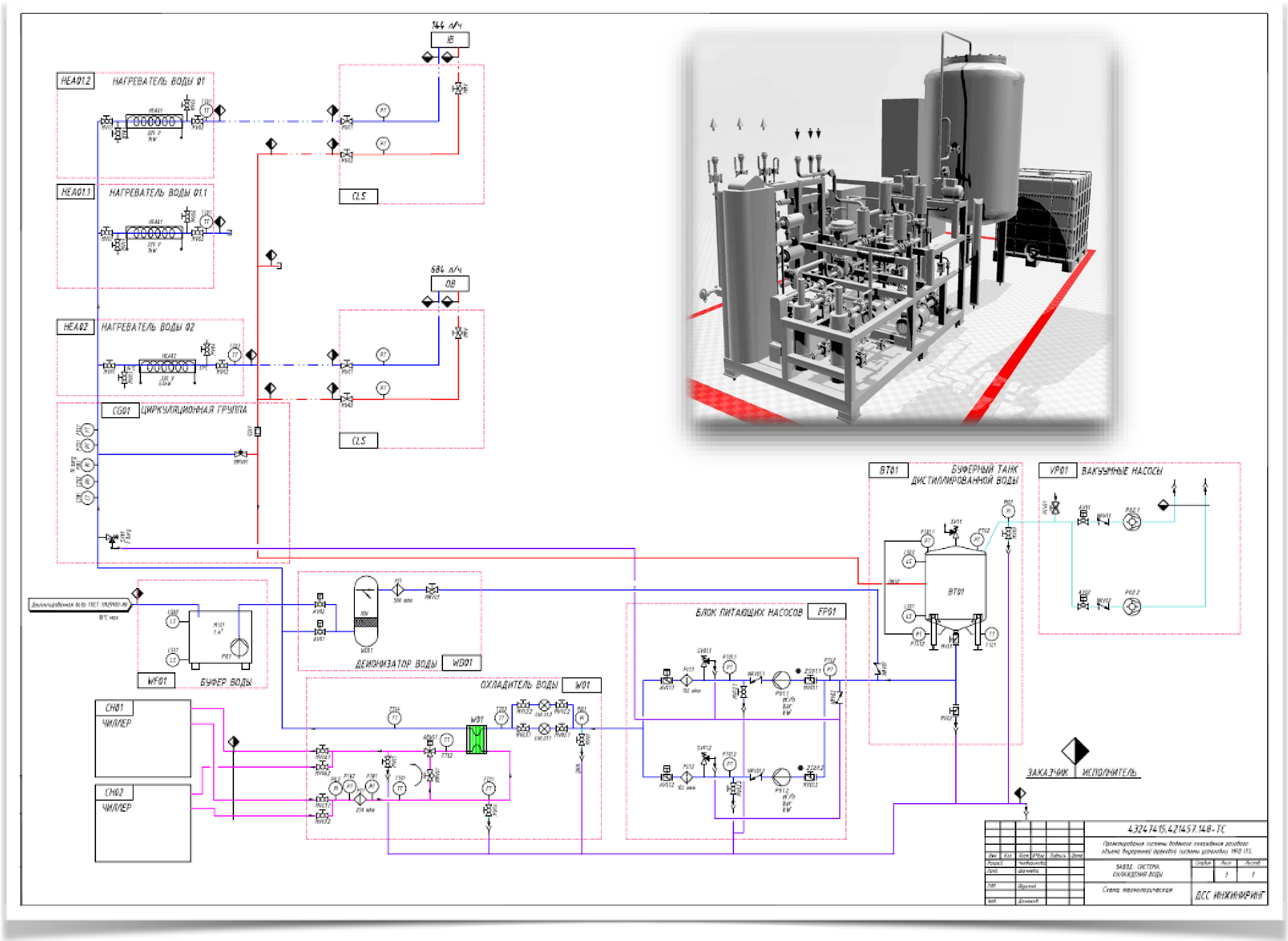
Ultrasonic bonding Chips - FPC



HIC testing

A.Sheremetiev with T.Andreeva, S.Patronova,T.Semchukova and C/Ceballos

Cooling Plant by DSSE for leakless water cooling system



Barrel type	No. of Staves	No. of Panels	No. of Circuits	Power in the circuit [W]	Flow [l/h]
IB	96	96	24	240	288
OB	54	108	9	2187	684
Total ITS	150	204	33	2427	972

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- Delivery of instrumentation and control equipment (Dec. 2024).
- Production and tests.

Conclusions and outlook

Milestones achieved:

- ✓ NICA MPD-ITS Consortium" has been established between JINR as Russian coordination center and CCNU as China coordination center with the acting time of 5 years.
- ✓ Installation Container is 90% ready.
- ✓ MICA first prototype was produced and passed testing.
- ✓ Power Board are ready for mass production.

Plans:

- Proceed with integration of Installation Container into TPC in October 2025.
- Finalize FPGA and ACIS-based Readout Unit .
- Finalize MICA chip design. MICA chip serial production will start in 2027 according to the current plan.
- MPD ITS in “OB-only” configuration (42 staves, three layers) is planned to be commissioned roughly in 2028.

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